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Requirements and Compatibility | Ordering Information | Detailed Specifications
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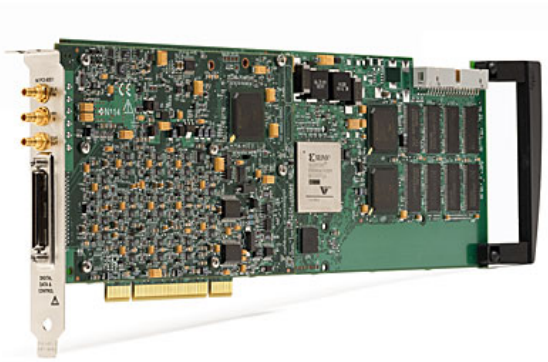
Last Revised: 2012-08-06 09:57:39.0

NI PXI-6551, NI PCI-6551, NI PXI-6552, NI PCI-6552



Overview

NI 6551 and NI 6552 are 50/100 MHz digital waveform generator/analyzers. They feature 20 channels with programmable voltage levels and per-clock-cycle, per-channel direction control. The devices offer deep onboard memory with triggering and pattern sequencing. The latest version of NI-HSDIO driver software adds the ability to perform immediate comparisons of expected data with acquired response data. With these features, you can implement a wide range of digital stimulus-response applications, such as functional testing of memory chips and bidirectional communication.

The NI Digital Waveform Editor is an interactive software tool that you can use with NI 6551/52 devices to quickly and easily create, edit, and import digital waveforms. NI includes the Digital Waveform Editor free of charge with the 8 and 64 Mbit/channel models.

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Requirements and Compatibility

OS Information

- Windows 7
- Windows 7 64-bit
- Windows Vista x64/x86

Driver Information

- NI-HSDIO

Software Compatibility

- ANSI C/C++
- LabVIEW
- LabWindows/CVI
- Measurement Studio

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Application and Technology

Design High-Performance Tests

For building high-performance stimulus-response systems, the NI 655x devices include the following:

- A sophisticated timing engine to adjust for the timing parameters of the device under test
- Programmable voltage levels for testing multiple devices or characterizing a single device under changing conditions
- Per-cycle tristate for bidirectional communication
- A versatile memory architecture for maximum flexibility of waveform and scripting memory

The hardware architecture is designed to preserve high signal quality, and an eye diagram of the PXI-6552 generation is shown in Figure 1.

You can use the internal clock or an external clock, such as from the NI PXI-5404, through the front panel. You can also shift the data generated, data acquired, and exported sample clock relative to the onboard clock for clock frequencies above 25 MHz, which is critical to adjust for propagation delays and setup-and-hold times in the device under test.

You need programmable voltage levels when testing different devices or when characterizing how a given device performs under changing conditions. With NI 655x devices, you can set the high and low levels for acquisition and generation independently. You can program the voltage levels between -2.0 and 5.5 V with 10 mV resolution for TTL, LVTTL, LVCMOS, ECL, PECL, and other signal-level compatibility.

The SMC memory architecture is designed for maximum flexibility between waveform memory and scripting memory. Using a single memory bank, you can allocate as much memory as you need for script and waveform data, giving you maximum flexibility from test to test.

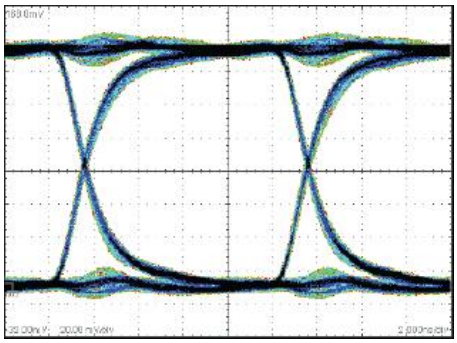

Figure 1. Eye Diagram of NI PXI-6552 Generation

Create Digital Waveforms Interactively with the NI Digital Waveform Editor

With the NI Digital Waveform Editor, an interactive software tool for creating and editing digital waveforms, you can import existing test patterns from popular spreadsheet and VHDL simulation packages in ASCII or value change dump (VCD) formats. Once imported, you can view the waveforms graphically and edit them interactively for new devices or new test conditions. You can also build new waveforms with built-in fill patterns such as pseudorandom bit sequences (PRBS) and count up/down patterns. When you are ready to test your device, the waveforms import seamlessly into NI LabVIEW, LabVIEW SignalExpress, and C. The Digital Waveform Editor is included with the 8 and 64 Mbit/channel memory models, and is a separate add-on for use with the 1 Mbit/channel model.

Build Tightly Synchronized Mixed-Signal Test Systems

NI 655x devices use the same SMC architecture as the NI 5122 high-resolution digitizers and NI 5441 arbitrary waveform generators, so you can combine these devices to build tightly synchronized mixed-signal prototyping and test systems. For tight timing requirements, these PXI modules phase-lock to the 10 MHz reference clock on the PXI backplane. If you have an external precision reference, you can import it through the front panel SMB connector.

Driver Software

NI 655x devices include the NI-HSDIO driver with an intuitive, powerful API based on IVI guidelines. The Windows-compatible NI-HSDIO driver provides an API for LabVIEW, LabVIEW SignalExpress, LabWindows™/CVI, and other text-based development environments.

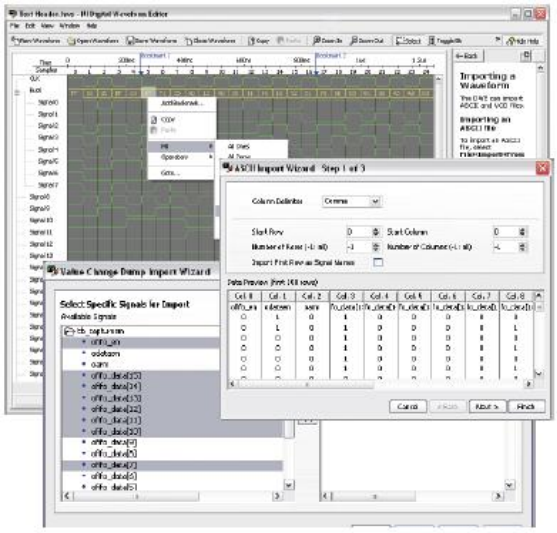

Figure 2. NI Digital Waveform Editor with ASCII and VCD Import Wizards

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Ordering Information

For a complete list of accessories, visit the product page on ni.com.

Products	Part Number	Recommended Accessories	Part Number
NI PCI-6551			
NI PCI-6551- 1 Mb/ch Each NI PCI-6551- 1 Mb/ch requires: 1 Connector Block	778950-01	No accessories required.	
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PCI-6551			
NI PCI-6551- 8 Mb/ch	778950-02	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m)	196275-01

Each NI PCI-6551- 8 Mb/ch requires: 1 Cable, 1 Connector Block		***Also available: Shielded*	
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PCI-6552			
NI PCI-6552- 64 Mb/ch Each NI PCI-6552- 64 Mb/ch requires: 1 Cable, 1 Connector Block	778951-03	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PCI-6552			
NI PCI-6552- 8 Mb/ch Each NI PCI-6552- 8 Mb/ch requires: 1 Cable, 1 Connector Block	778951-02	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXI-6551			
NI PXI-6551-1 Mb/ch Each NI PXI-6551-1 Mb/ch requires: 1 Cable, 1 Connector Block	778538-01	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXI-6551			
NI PXI-6551-64 Mb/ch Each NI PXI-6551-64 Mb/ch requires: 1 Cable, 1 Connector Block	778538-03	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXI-6551			
NI PXI-6551-8 Mb/ch Each NI PXI-6551-8 Mb/ch requires: 1 Cable, 1 Connector Block	778538-02	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXI-6552			
NI PXI-6552-1 Mb/ch Each NI PXI-6552-1 Mb/ch requires: 1 Cable, 1 Connector Block	778539-01	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXI-6552			
NI PXI-6552-64 Mb/ch Each NI PXI-6552-64 Mb/ch requires: 1 Cable, 1 Connector Block	778539-03	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXI-6552			
NI PXI-6552-8 Mb/ch Each NI PXI-6552-8 Mb/ch requires: 1 Cable, 1 Connector Block	778539-02	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01

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Support and Services

System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

Calibration

NI measurement hardware is calibrated to ensure measurement accuracy and verify that the device meets its published specifications. To ensure the ongoing accuracy of your measurement hardware, NI offers basic or detailed recalibration service that provides ongoing ISO 9001 audit compliance and confidence in your measurements. To learn more about NI calibration services or to locate a qualified service center near you, contact your local sales office or visit ni.com/calibration.

Technical Support

Get answers to your technical questions using the following National Instruments resources.

- **Support** - Visit ni.com/support to access the NI KnowledgeBase, example programs, and tutorials or to contact our applications engineers who are located in NI sales offices around the world and speak the local language.
- **Discussion Forums** - Visit forums.ni.com for a diverse set of discussion boards on topics you care about.
- **Online Community** - Visit community.ni.com to find, contribute, or collaborate on customer-contributed technical content with users like you.

Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

Training and Certifications

The NI training and certification program delivers the fastest, most certain route to increased proficiency and productivity using NI software and hardware. Training builds the skills to more efficiently develop robust, maintainable applications, while certification validates your knowledge and ability.

- **Classroom training in cities worldwide** - the most comprehensive hands-on training taught by engineers.
- **On-site training at your facility** - an excellent option to train multiple employees at the same time.
- **Online instructor-led training** - lower-cost, remote training if classroom or on-site courses are not possible.
- **Course kits** - lowest-cost, self-paced training that you can use as reference guides.
- **Training memberships** and training credits - to buy now and schedule training later.

Visit ni.com/training for more information.

Extended Warranty

NI offers options for extending the standard product warranty to meet the life-cycle requirements of your project. In addition, because NI understands that your requirements may change, the extended warranty is flexible in length and easily renewed. For more information, visit ni.com/warranty.

OEM

NI offers design-in consulting and product integration assistance if you need NI products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

Alliance

Our Professional Services Team is comprised of NI applications engineers, NI Consulting Services, and a worldwide National Instruments Alliance Partner program of more than 700 independent consultants and integrators. Services range from start-up assistance to turnkey system integration. Visit ni.com/alliance.

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Detailed Specifications

This document provides the specifications for the NI PXI/PCI-6551 (NI 6551) and the NI PXI/PCI-6552 (NI 6552), collectively called the NI 655*X*.

Typical values are representative of an average unit operating at room temperature. Specifications are subject to change without notice. For the most recent NI 6551/6552 specifications, visit *ni.com/manuals*.

To access the NI 655*X* documentation, including the *NI Digital Waveform Generator/Analyzer Getting Started Guide*, which contains functional descriptions of the NI 655*X* signals, navigate to **Start » Programs » National Instruments » NI-HSDIO » Documentation**.

Hot Surface If the NI 655*X* has been in use, it may exceed safe handling temperatures and cause burns. Allow time to cool before removing it from the chassis.

Channel Specifications

Specification	Value	Comments
Number of data channels	20	—
Direction control of data channels	Per channel	—

Specification	Value	Comments
Number of Programmable Function Interface (PFI) channels	4	Refer to the *Waveform Characteristics* section for more details.
Direction control of PFI channels	Per channel	—
Number of clock terminals	3 input, 2 output	Refer to the *Timing Specifications* section for more details.

Generation Channels (Data, DDC CLK OUT, and PFI <0:3>)

Specification	Value		Comments
Generation voltage range	–2.0 V to 5.5 V		Into 1 MΩ
Generation signal type	Single-ended		—
Number of programmable voltage levels	1 voltage low level 1 voltage high level **Note** While you can only set one voltage low level and one voltage high level for all generation channels, you can set a different voltage low level and voltage high level for all acquisition channels.		For all data, CLK OUT (Sample clock only), and PFI channels
Generation voltage range restrictions	–0.5 V to 5.5 V (up to 50 MHz clock rate) –2.0 V to 3.7 V (up to 50 MHz clock rate) –0.5 V to 3.7 V (50 to 100 MHz clock rate; NI 6552 only)		Into 1 MΩ
Generation voltage swing	400 mV to 6 V (up to 50 MHz clock rate) 400 mV to 4.2 V (50 to 100 MHz clock rate; NI 6552 only)		Into 1 MΩ
Generation voltage level resolution	10 mV		Into 1 MΩ
DC generation voltage level accuracy	±20 mV		Into 1 MΩ; does not include system crosstalk
Output impedance	50 Ω nominal		At 25 °C
Output impedance temperature coefficient	0.2 Ω/°C		Typical
Maximum DC drive strength	±50 mA maximum per channel ±600 mA maximum for all data, clock, and PFI channels		—
Data channel driver enable/disable control	Per channel		Software- selectable
Channel power-up state	**Module Assemblies Labeled A and B**	**Module Assemblies Labeled C and Later**	—
	Drivers disabled, 10 kΩ input impedance	Drivers disabled, 50 kΩ input impedance	
Output protection	The device can indefinitely sustain a short to any voltage in the generation voltage range.		—

Acquisition Channels (Data, STROBE, and PFI <0..3>)

Specification	Value	Comments
Number of voltage comparators per channel	2	—
Acquisition voltage range	–2.0 V to 5.5 V	—
Number of programmable acquisition thresholds	1 voltage low threshold 1 voltage high threshold **Note** While you can set only one voltage low level and one voltage high level for all acquisition channels, you can set a different voltage low level and voltage high level for all generation channels.	For all data, STROBE, and PFI channels
Minimum detectable voltage swing	50 mV	10 kΩ input impedance, measured with 50% duty cycle input signal
Acquisition voltage threshold resolution	10 mV	10 kΩ input impedance
DC acquisition voltage	±30 mV	10 kΩ input impedance, does not include

Specification	Value		Comments
threshold accuracy			system crosstalk
Input impedance	**Module Assemblies Labeled A and B**	**Module Assemblies Labeled C and Later**	Software-selectable per channel when powered on and within valid voltage range.
	50 Ω nominal or 10 kΩ (default)	50 Ω nominal or 50 kΩ (default)	
Input protection	–2.3 V to 6.8 V		Diode clamps in the design may provide additional protection outside this range.

Timing Specifications

Sample Clock

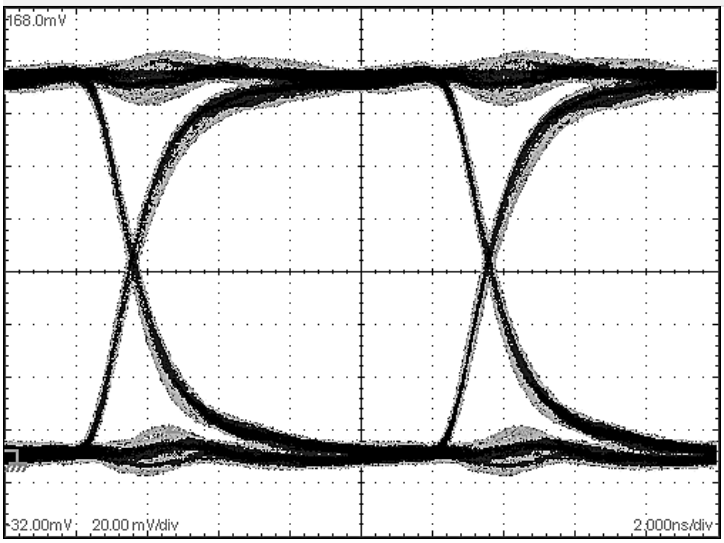
Specification	Value		Comments
Sample clock sources	1. On Board Clock (internal voltage-controlled crystal oscillator (VCXO) with divider) 2. CLK IN (SMB jack connector) 3. PXI_STAR (PXI backplane—PXI only) 4. STROBE (DDC connector; acquisition only)		—
On Board Clock frequency range	**NI 6551:** 48 Hz to 50 MHz Configurable to 200 MHz / *N*, where 4 ≤ *N* ≤ 4,194,304 **NI 6552:** 48 Hz to 100 MHz Configurable to 200 MHz / *N*, where 2 ≤ *N* ≤ 4,194,304		—
CLK IN frequency range	NI 6551: 20 kHz to 50 MHz NI 6552: 20 kHz to 100 MHz		Refer to the *CLK IN (SMB Jack Connector)* section for restrictions based on waveform type.
PXI_STAR frequency range (PXI only)	NI 6551: 48 Hz to 50 MHz NI 6552: 48 Hz to 100 MHz		Refer to the *PXI_STAR (PXI Backplane—PXI only)* section.
STROBE frequency range	NI 6551: 48 Hz to 50 MHz NI 6552: 48 Hz to 100 MHz		Refer to the *STROBE (DDC Connector)* section.
Sample clock relative delay adjustment	0.0 to 1.0 Sample clock periods		You can apply a delay or phase adjustment to the On Board Clock to align multiple devices.
Sample clock relative delay adjustment resolution	10 ps		
Exported Sample clock destinations	1. DDC CLK OUT (DDC connector) 2. CLK OUT (SMB jack connector)		Sample clocks with sources other than STROBE can be exported.
Exported Sample clock delay range (δ_C)	0.0 to 1.0 Sample clock periods		For clock frequencies ≥25 MHz
Exported Sample clock delay resolution (δ_C)	1/256 of Sample clock period		For clock frequencies ≥25 MHz
Exported Sample clock jitter	**Period Jitter**	**Cycle-to-Cycle Jitter**	Typical; using On Board Clock
	20 ps_{rms}	35 ps_{rms}	

Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)

Specification	Value	Comments
Data channel-to- channel skew	±300 ps	Typical skew across all data channels
	±900 ps	Maximum skew across all data channels
Maximum data channel toggle rate	**NI 6551:** 25 MHz **NI 6552:** 50 MHz	—
Data formats	NRZ	—
Data position modes	Sample Clock Rising Edge, Sample Clock Falling Edge, or Delay from Sample Clock Rising	Per channel

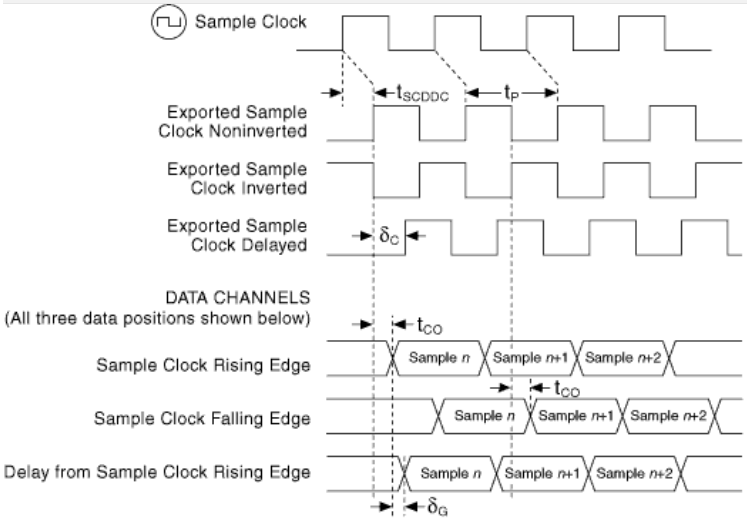
Specification	Value	Comments
	Edge	
Generation data delay range (δ_G)	0.0 to 1.0 Sample clock periods	Supported for clock frequencies ≥25 MHz
Generation data delay resolution (δ_G)	1/256 of Sample clock period	Supported for clock frequencies ≥25 MHz

Eye Diagram [1]



Specification	Value		Comments
Rise time (0 V to 3.3 V swing)	Into 50 Ω	2.25 ns	20% to 80%, typical
	Into 1 MΩ	2.75 ns into 475 pF test system capacitance	
Fall time (0 V to 3.3 V swing)	Into 50 Ω	2.25 ns	20% to 80%, typical
	Into 1 MΩ	2.75 ns into 475 pF test system capacitance	
Exported Sample clock offset (t_{CO})	0 ns or 2.5 ns (default)		Software-selectable
Time delay from Sample clock (internal) to DDC connector (t_{SCDDC})	32.5 ns		Typical

Generation Timing Diagram



t_{SCDDC} : Time delay from Internal Sample Clock to DDC Connector Exported Sample Clock

$0 \le \delta_C \le 1$: Exported Sample Clock Delay (fraction of t_P)

$0 \le \delta_G \le 1$: Generation Data Delay (fraction of t_P)

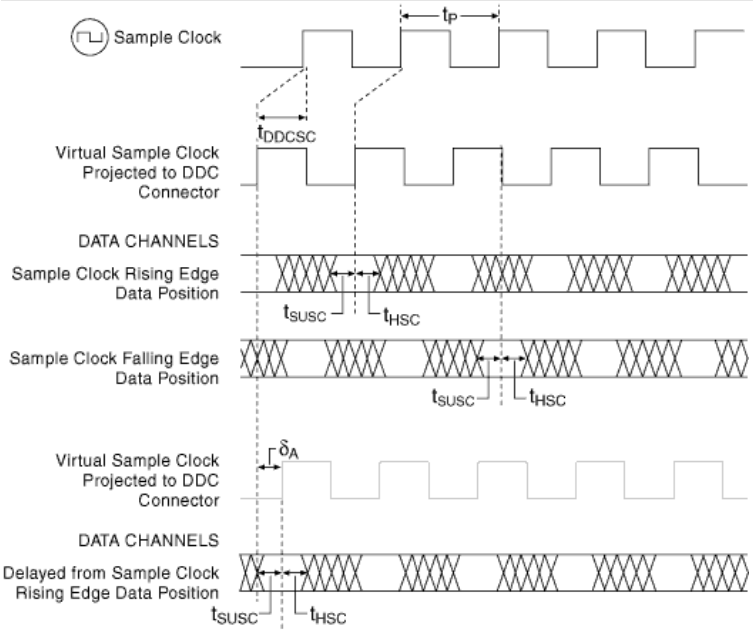
$t_P = \frac{1}{f}$ = Sample Clock Period

t_{CO} = Exported Sample Clock Offset; 0 or 2.5 ns, software-selectable

Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)

Specification	Value	Comments
Channel-to- channel skew	±400 ps	Typical skew across all data channels
	±900 ps	Maximum skew across all data channels
Minimum detectable pulse width	4 ns	Required at both acquisition voltage thresholds
Set-up time to STROBE (t_{SUS})	2.3 ns	Maximum; includes maximum data channel-to-channel skew
Hold time to STROBE (t_{HS})	1.9 ns	Maximum; includes maximum data channel-to-channel skew
Time delay from DDC connector to internal Sample clock (t_{DDCSC})	27.5 ns	Typical
Set-up time to Sample clock (t_{SUSC})	0.4 ns	Does not include data channel-to- channel skew, t_{DDCSC}, or t_{SCDDC}
Hold time to Sample clock (t_{HSC})	0 ns	Does not include data channel-to- channel skew, t_{DDCSC}, or t_{SCDDC}
Data position modes	Sample Clock Rising Edge, Sample Clock Falling Edge, or Delay from Sample Clock Rising Edge	Per channel
Acquisition data delay range (δ_A)	0.0 to 1.0 Sample clock periods	For clock frequencies ≥25 MHz
Acquisition data delay resolution (δ_A)	1/256 of Sample clock period	For clock frequencies ≥25 MHz

Acquisition Timing Diagram



t_{DDCSC} : Time Delay from DDC Connector to Internal Sample Clock

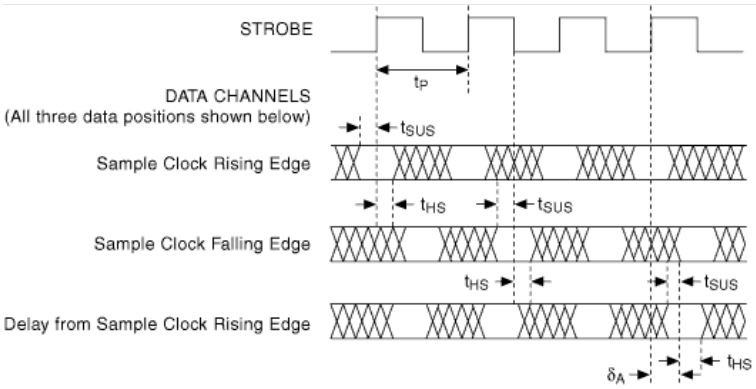
$0 \le \delta_A \le 1$: Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{SUSC} = Set-Up Time to Sample Clock

t_{HSC} = Hold Time to Sample Clock

Acquisition Timing Diagram Using STROBE as the Sample Clock



t_{SUS} = Set-Up Time to STROBE

t_{HS} = Hold Time from STROBE

$0 \le \delta_A \le 1$: Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Sample Clock Period

CLK IN (SMB Jack Connector)

Specification	Value				Comments
Direction	Input into device				—
Destinations	1. Reference clock (for the phase lock loop (PLL)) 2. Sample clock				—
Input coupling	AC				—
Input protection	±10 VDC				—
Input impedance	50 Ω (default) or 1 kΩ				Software-selectable
Minimum detectable pulse width	4 ns				Required at V_{rms} mean
Clock requirements	Clock must be continuous and free-running				—
As Sample clock					
External Sample clock requirements	**Square Waves**				—
	Voltage range	0.65 V_{pp} to 5.0 V_{pp}			—
	Frequency range	**NI 6551:** 20 kHz to 50 MHz			—
		NI 6552: 20 kHz to 100 MHz			—
	Duty cycle range	f < 50 MHz: 25% to 75% f ≥ 50 MHz: 40% to 60%			—
	Sine Waves				—
	Voltage range	0.65 V_{pp} to 5.0 V_{pp}	1.0 V_{pp} to 5.0 V_{pp}	2.0 V_{pp} to 5.0 V_{pp}	—
	Frequency range	**NI 6551:** 5.5 MHz to 50 MHz	**NI 6551:** 3.5 MHz to 50 MHz	**NI 6551:** 1.8 MHz to 50 MHz	—
		NI 6552: 5.5 MHz to 100 MHz	**NI 6552:** 3.5 MHz to 100 MHz	**NI 6552:** 1.8 MHz to 100 MHz	—
As Reference Clock					
Reference clock frequency range	10 MHz ±50 ppm				—
Reference clock voltage range	0.65 V_{pp} to 5.0 V_{pp}				—
Reference clock duty cycle	25% to 75%				—

STROBE (DDC Connector)

Specification	Value	Comments
Direction	Input into device	—
Destinations	Sample clock (acquisition only)	—
STROBE frequency range	**NI 6551:** 48 Hz to 50 MHz **NI 6552:** 48 Hz to 100 MHz	—

Specification	Value		Comments
STROBE duty cycle range	**NI 6551:** 25% to 75% **NI 6552:** $f \leq$ 50 MHz: 25% to 75% $f >$ 50 MHz: 40% to 60%		At the programmed thresholds
Minimum detectable pulse width	4 ns		Required at both acquisition voltage thresholds
Voltage thresholds	Refer to the *Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)* specifications in the *Channel Specifications* section.		—
Clock requirements	Clock must be continuous and free-running		—
Input impedance	**Module Assemblies Labeled A and B**	**Module Assemblies Labeled C and Later**	Software-selectable
	50 Ω or 10 kΩ (default)	50 Ω or 50 kΩ (default)	

PXI_STAR (PXI Backplane—PXI only)

Specification	Value	Comments
Direction	Input into device	—
Destinations	1. Sample clock 2. Start trigger 3. Reference trigger (acquisition sessions only) 4. Advance trigger (acquisition sessions only) 5. Pause trigger (generation sessions only) 6. Script trigger (generation sessions only)	—
PXI_STAR frequency range	**NI 6551:** 48 Hz to 50 MHz **NI 6552:** 48 Hz to 100 MHz	—
Clock requirements	Clock must be continuous and free-running	—

CLK OUT (SMB Jack Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)	—
Output impedance	50 Ω nominal	—
As Sample Clock		
Electrical characteristics	Refer to the *Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)* specifications in the *Channel Specifications* section.	—
As Reference Clock		
Maximum drive current	24 mA	—
Logic type	3.3 V CMOS	—

DDC CLK OUT (DDC Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	Sample clock	STROBE cannot be routed to DDC CLK OUT
Electrical characteristics	Refer to the *Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)* specifications in the *Channel Specifications* section.	—

Reference Clock (PLL)

Specification	Value	Comments
Reference clock sources	1. PXI_CLK10 (PXI backplane—PXI only) 2. RTSI 7 (RTSI bus—PCI only) 3. CLK IN (SMB jack connector) 4. None (On Board Clock not locked to a reference)	Provides the reference frequency for the PLL
Lock time	400 ms	Typical
Reference clock frequencies	10 MHz ±50 ppm	—
Reference clock duty cycle	25% to 75%	—
Reference clock destinations	CLK OUT (SMB jack connector)	—

Waveform Characteristics

Memory and Scripting

Specification	Value			Comments
Memory architecture	The NI 655*X* uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user-defined.			Refer to the *NI Digital Waveform Generator/ Analyzer Help* for more information.
Onboard memory size	1 Mbit/channel (for generation sessions) 1 Mbit/channel (for acquisition sessions)	8 Mbit/channel (for generation sessions) 8 Mbit/channel (for acquisition sessions)	64 Mbit/channel (for generation sessions) 64 Mbit/channel (for acquisition sessions)	Maximum limit for generation sessions assumes no scripting instructions.
Generation modes	**Single-waveform mode:** Generate a single waveform once, *N* times, or continuously.			—
	Scripted mode: Generate a simple or complex sequence of waveforms. Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script triggers.			
Generation minimum waveform size	**Configuration**	**Sample Rate**		Sample rate dependent. Increasing sample rate increases minimum waveform size requirement. For information on these configurations, refer to the *Common Scripting Use Cases* topic in the *NI Digital Waveform Generator/ Analyzer Help*.
		100 MHz (NI 6552 only)	**50 MHz**	
	Finite waveform	2 S	2 S	
	Continuous waveform	32 S	16 S	
	Stepped triggered script	128 S	64 S	
	Burst triggered script	512 S	256 S	
Generation finite repeat count	1 to 16,777,216			—
Generation waveform quantum	Waveform size must be an integer multiple of 2 S.			Regardless of waveform size, NI-HSDIO allocates waveforms into block sizes of 32 S of physical memory.
Acquisition minimum record size	1 S			—
Acquisition record quantum	1 record			—
Acquisition number of pre-Reference trigger samples	0 up to full record			—
Acquisition number of post-Reference trigger samples	0 up to full record			—

Triggers (Inputs to the NI 655*X*)

Specification	Values	Comments
Trigger types	1. Start trigger 2. Pause trigger	—

Specification	Values			Comments
	3. Script trigger (generation sessions only) 4. Reference trigger (acquisition sessions only) 5. Advance trigger (acquisition sessions only)			
Sources	1. PFI 0 (SMB jack connector) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..7> (PXI backplane—PXI only)/ RTSI <0..7> (RTSI bus—PCI only) 4. PXI_STAR (PXI backplane—PXI only) 5. Pattern match (acquisition sessions only) 6. Software (user function call) 7. Disabled (do not wait for a trigger)			—
Trigger detection	1. Start trigger (edge detection: rising or falling) 2. Pause trigger (level detection: high or low) 3. Script trigger <0..3> (edge detection: rising or falling; level detection: high or low) 4. Reference trigger (edge detection: rising or falling) 5. Advance trigger (edge detection: rising or falling)			—
Minimum required trigger pulse width	**Generation Triggers**	**Acquisition Triggers**		—
	30 ns	Acquisition triggers must meet set-up and hold time requirements.		
Trigger rearm time	**Start to Reference Trigger**	**Start to Advance Trigger**	**Reference to Reference Trigger**	—
	57 S, typical; 64 S maximum	138 S, typical; 143 S, maximum	132 S, typical; 153 S, maximum	
Destinations	1. PFI 0 (SMB jack connectors) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..7> (PXI backplane—PXI only)/ RTSI <0..7> (RTSI bus—PCI only)			Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported for acquisition sessions.
Delay from Pause trigger to Paused state	**Generation Sessions**	**Acquisition Sessions**		—
	32 Sample clock periods + 150 ns	Synchronous to the data		Use the Data Active event during generation to determine when the NI 655*X* enters the Pause state.
Delay from trigger to digital data output	32 Sample clock periods + 160 ns			—

Events (Output from the NI 655*X*)

Specification	Value	Comments
Event type	1. Marker <0..3> (generation sessions only) 2. Data Active event (generation sessions only) 3. Ready for Start event 4. Ready for Advance event (acquisition sessions only) 5. End of Record event (acquisition sessions only)	—
Destinations	1. PFI 0 (SMB jack connectors) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..7> (PXI backplane—PXI only)/ RTSI <0..7> (RTSI bus—PCI only)	Each event, except the Data Active event, can be routed to any destination. The Data Active event can only be routed to PFI channels.
Marker time resolution (placement)	Markers must be placed at an integer multiple of 2 S	—

Calibration

Specification	Value	Comments
Interval for external calibration	2 years	—
Warm-up time	15 minutes	—
Onboard calibration voltage reference		
Temperature coefficient	±5 ppm/°C	—
Long-term stability	90 ppm /√ kHr	Typical
On Board Clock characteristics (only valid when PLL reference source is set to None)		
Frequency accuracy	±100 ppm	Typical
Temperature stability	±30 ppm	Typical
Aging	±5 ppm first year	Typical

Power

Specification	Value			Comments
	Typical	Maximum		
+3.3 VDC	2.0 A	2.0 A		—
+5 VDC	1.8 A	**PXI**	**PCI**	—
		2.3 A	2.4 A	—
+12 VDC	0.3 A	0.5 A		—
–12 VDC	0.2 A	0.2 A		—
Total power	21.6 W	**PXI**	**PCI**	—
		26.5 W	27 W	—

Software Specifications

Specification	Value	Comments
Driver software	NI-HSDIO driver software. NI-HSDIO allows you to configure, control, and calibrate the NI 655*X*. NI-HSDIO provides application interfaces for many development environments. NI-HSDIO follows IVI API guidelines.	—
Application software	NI-HSDIO provides programming interfaces for the following application development environments: National Instruments LabVIEW 7.0 or later National Instruments LabWindows™/CVI™ 6.0 or later Microsoft Visual C/C++ 6.0 or later	—
Test panel	National Instruments Measurement & Automation Explorer (MAX) provides test panels with basic acquisition and generation functionality for the NI 655*X*. MAX is included on the NI-HSDIO driver CD.	—

Environment

Note To ensure that the NI 655*X* cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included with the NI 655*X*. The NI 655*X* is intended for indoor use only.

Specification	Value		Comments
Operating temperature	**PXI**	**PCI**	
	0 °C to +55 °C in all NI PXI chassis except the following: 0 °C to +45 °C when installed in an NI PXI-1000/B and NI PXI-101*X* chassis (Meets IEC-60068-2-1 and IEC-60068-2-2)	0 °C to +45 °C	—
Storage temperature	–20 °C to 70 °C		—
Operating relative humidity	10% to 90% relative humidly, noncondensing (Meets IEC-60068-2-56)		—
Storage relative humidity	5% to 95% relative humidity, noncondensing (Meets IEC-60068-2-56)		—

Specification	Value	Comments
Operating shock	30 g, half-sine, 11 ms pulse (Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	NI PXI-655*X* only
Storage shock	50 g, half-size, 11 ms pulse (Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	NI PXI-655*X* only
Operating vibration	5 Hz to 500 Hz, 0.31 g_{rms} (Meets IEC-60068-2-64)	NI PXI-655*X* only
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (Meets 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B)	NI PXI-655*X* only
Altitude	0 m to 2,000 m above sea level (at 25 °C ambient temperature)	—
Pollution Degree	2	—

Safety, Electromagnetic Compatibility, and CE Compliance

Specification	Value	Comments
Safety	The NI 655*X* meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use: ▪ IEC 61010-1, EN 61010-1 ▪ UL 3111-1, UL 61010B-1 ▪ CAN/CSA-C22.2 No. 1010-1	For UL and other safety certifications, refer to the product label or to ni.com.
Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz	—
Immunity	EN 61326:1997 + A2:2001, Table 1	—
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant **Note** For EMC compliance, you *must* operate this device with shielded cabling.	—
This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:		
Low-Voltage Directive (safety)	73/23/EEC	—
Electromagnetic Compatibility Directive (EMC)	89/336/EEC	—
For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.		

Physical Specifications

Specification	Value		Comments
Dimensions	**PXI**	**PCI**	
	18.6 cm × 13.1 cm (7.32 in. × 5.16 in.) Single 3U CompactPCI slot; PXI compatible	12.6 cm × 35.5 cm (4.95 in. × 13.9 in.)	—
Weight	375 g (13.2 oz)		—
Front Panel Connectors			
Label	**Function(s)**	**Connector Type**	—
CLK IN	External Sample clock, external PLL reference input	SMB jack connector	—
PFI 0	Events, triggers	SMB jack connector	—
CLK OUT	Exported Sample clock, exported Reference clock	SMB jack connector	—
DIGITAL DATA & CONTROL	Digital data channels, exported Sample clock, STROBE, events, triggers	68-pin VHDCI connector	—

[1] This eye diagram was captured on DIO 0 (100 MHz clock rate) at 3.3 V at room temperature into 50 Ω termination.

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