A ASA 312 and NAA I Specifications

Overview

This appendix provides a summary of ASA 312, NAA I, and protocol processor features and specifications.

IMPORTANT ➤
Specifications are subject to change without notice.➤

ASA 312 Features

The following states various ASA 312 features.

ASA 312 Features	
Calibration	Allows in-the-field calibration. Eliminates the need to return unit for calibration. Two-year calibration interval period.
Color Touch Screen Display	High resolution VGA color touch screen .Extremely easy-to-use, menu-driven graphical user interface. User interface is controlled by either touch screen or mouse.
Five Independent Test Sets in One Unit	Complete DS1, E1, DS3, SONET, and ATM test sets in one portable unit. Each test set can be used independently and simultaneously.
Portable	Small light-weight design: 10.5 lbs (4.8 kg). OC-48 Configuration: 14 lbs (6.4 kg)
Printing	Prints all data and graphic screens.Supports HP LaserJet, HP ThinkJet, IBM ProPrinter, Epson FX, Seiko DPU-411, ASCII.
Programmable Testing	Allows programming of criteria and time interval for Pass/Fail testing. All settings and programs can be saved/recalled for repeated in-the-field testing.
Remote Access	Serial, Modem, or Ethernet: Remotes all functions to PC via serial or modem connection. PC software provides the identical screens with mouse input control.
Save/Recall	Allows Storage and Recall of test set's current results (every screen).
Software Upgrades	Users field upgradeable via serial port, modem, or Ethernet connection.
Switch Matrix	Cross-connects and multiplexes independent test sets internally via a patented switching fabric providing true control of multiple test sets in one unit.

Physical Characteristics

The following describes the ASA 312's physical characteristics.

Physical Characteristics	
Dimensions	10.1" H x 12.3" W x 4.7' D (257mm H x 312mm W x 120mm D)
Operating Temperature	0° to 50° C @ 85% Relative Humidity (RH) 0° to 40° C @ 85% RH with OC-48 configuration
Storage Temperature	-20° to 60° C @ 95% RH
Power Requirement	100–240 VAC, 48–65 Hz, 60 watts, 1.5 amps max. 90–132, 180–260 VAC, 47–63 Hz, 95 watts with OC-48 configuration
Weight:	10.5 lbs (4.8kg) 14.0 lbs (6.4kg) with OC-48 configuration

Auxiliary Interfaces

The following states the various connectors and interfaces available on the ASA 312's connector panel. Connectors will vary based on your hardware configuration.

Auxiliary Interfaces	
10baseT	8-pin modular jack, Ethernet 10Base-T Interface
Bits Clock	Bantam, Complies with AT&T CB119 and Pub 43802
DCC (DataCom Drop/Insert)	RS-449, DB-37 pin female connector for D1 through D12 Overhead bytes
External Trigger	BNC, TTL level input
GPIB	IEEE 488.2 Controller, Meets ANSI/IEEE 488.1-1987, IEC 624
Orderwire	4-pin modular jack for E1 or E2 bytes. Not intended for direct connection to telecommunications circuits
Parallel Port	RS-232, DB-25 pin female connector for parallel printer
PCMCIA	Type II PC Card slot for PC Card modem or SRAM Flash card.
RS-232	RS-232, DB-9 pin male connector for mouse, modem, direct connection or printer

NAA I Technical Specifications

This following is a list of technical specifications for the NAA I.

Specifications	Description
Approvals	This product is designed and conforms to NEBS Level 3 criteria per Bellcore SR-3580, tested per GR-63-CORE and GR-1089-CORE requirements.
Environment	
Operating Temperature	0° to 55° C at 85% relative humidity
Storage Temperature	-20° to 60° C at 95% relative humidity
Power Requirements	250 W max., Voltage range -42 to -56 V DC input 168 W typical at 3.5 Amps, -48V DC input
Fuse Requirements	
Backplane Fuses	1.5 Amp, 250 VAC, 2AG Slo-Blo® fuse (18 fuses per backplane)
Power Supply Fuse	15 Amp, 125 VAC, 5 x 20 mm Slo-Blo® fuse (1 fuse per Power Supply)
Dimensions	
Weight	35 pounds (15.9 kg) when fully configured
Height	10.50 inches (6U)
Width	17.63 inches (without mounting brackets attached)
Depth	10.63 inches
Ventilation Clearance	1.75 inches (1U) **above** and **below** the NAA I unit
Physical Interfaces	
DS1	DSX level, wire wrap pins
DS3	DSX level, BNC connectors
Optical	FC-PC, SC-PC, or ST-PC connectors
OC-48 Optical	FC-PC connectors only
STS-1	BNC connectors
DCC	DB-9 female connector
BITS	BITS clock, wire wrap pins
Remote Interface	
Ethernet	RJ-45 8-pin modular, 10BaseT connector
Dial	DB-9 male connector
X.25	DB-25 male connector
Tx Frequency	
DS1	1.544 Mhz, ± 4.6 ppm (Stratum III)
DS3	44.736 Mhz, ± 12 ppm
SONET (OC-N)	N x 51.84 Mhz, ± 4.6 ppm (Stratum III)
STS-1	51.84 Mhz, ± 4.6 ppm (Stratum III)
Rx Frequency	
DS1	1.544 Mhz, ± 200 ppm
DS3	44.736 Mhz, ± 200 ppm
SONET(OC-N)	N x 51.84 Mhz, ± 50 ppm
STS-1	51.84 Mhz, ± 50 ppm

SONET Protocol Processor

The following shows the SONET protocol processor technical specification.

SONET	Technical Specifications
Alarm Detection	Section: OOF, LOF, LOS, Line: AIS-L, FERF-L, LOP Path: AIS-P, Yellow-P, Unequipped-P VT: LOP-V, AIS-V, Yellow-V, Unequipped-V STSX-1 only: BPV
Alarm Generation	Section: LOF, LOS Line: AIS-L, FERF-L Path: LOP-P, AIS-P, Yellow-P, UNEQ-P VT: LOP-V, AIS-V, Yellow-V, UNEQ-V
APS Commands	Support of linear- and ring-mode commands
Clock	Internal, Received SONET signal, Bits
Connectors	
OC-N	FC-PC (standard), ST-PC, SC-PC
STSX-1	BNC
DataCom Channel (DCC)	Allows full testing of DCC.
Transmit	User defined byte Section D/I Line D/I DCC-Section PRBS (2^{-7}-1) DCC-line PRBS (2^{-7}-1).
Receive (Drop from SONET)	Pattern Sync LED Bit Error LED Error Count BER Error Seconds.
Receive (Input from DCC connector)	Pattern Sync LED, Bit Error LED, Error Count, BER, Error Seconds.
Error Injection	Random, Section CV, Line CV, Path CV, VT CV, Path FEBE, VT FEBE, VT Random, Line FEBE, Payload Bit
Error Injection Rate	Single, 10^{-7} to 10^{-3}, User Programmable
Error Measurement	Section CV, Line CV, Path CV, VT CV, Path FEBE, VT FEBE, VT Random, Line FEBE, Payload Bit
Framing	STS-N A1 and A2 bytes
Frequency (N=1, 3, 12, or 48)	N x 51.84 Mhz, ± 2ppm (Tx), -1 ppm/yr N x 51.84 Mhz, ± 50ppm (Rx)
History Graphs	Errors and alarms are graphed over a user selected time period. Each test set can independently log data for up to three days (72 hours).
Impedance	STSX-1: 75 ohms ± 5% unbalanced

SONET	Technical Specifications
Input Jitter Tolerance:	
OC-1	10 Hz – 30 Hz, > 15 UI 30 Hz – 300 Hz, > 1.5 UI 300 Hz – 2 kHz, > 1.5 UI 2 kHz – 20 kHz, > 0.15 UI
OC-3	10 Hz – 30 Hz, > 15 UI 30 Hz – 300 Hz, > 1.5 UI 300 Hz – 6.5 kHz, > 1.5 UI 6.5 kHz – 75 kHz, > 0.15 UI
OC-12	10 Hz – 30 Hz, > 15 UI 30 Hz – 300 Hz, > 1.5 UI 300 Hz – 25 kHz, > 1.5 UI 25 kHz – 250 kHz,> 0.15 UI
STSX-1	10 Hz – 30 Hz, > 15 UI 30 Hz – 300 Hz, > 1.5 UI 300 Hz – 2 kHz, > 1.5 UI 2 kHz – 20 kHz, > 0.15 UI
Input Signal Measurement	
OC-N (N = 1, 3, or 12)	Optical Power Meter: 0 to -26 dBm, ± 1.5 dBm Frequency Measurement Range: N x 51.84 MHz, ± 50 ppm
OC-48	Optical Power Meter: 0 to -26 dBm, ± 1.5 dBm Frequency Measurement Range: 2488.32 MHz, ± 50 ppm
STSX-1	Peak positive and negative voltage range: ± 0.31Vp to ± 1.2Vp Frequency Measurement Range: N x 51.84 MHz, ± 50 ppm
Level Rx	
OC-N (N = 1, 3, or 12)	-7 to -26 dBm, -30 dBm typical min. at 10^{-10} BER with 2^{23}-1 PRBS
OC-48:	-2 dBm to -26 dBm

SONET	Technical Specifications
Level Tx	
OC-N (N =1, 3, or 12)	Optical 1310 nm: -5 dBm typical, single-mode, Intermediate Reach 1260 – 1360 nm, 1308 nm typical Optical 1550 nm: 0 dBm typical, single-mode, Intermediate Reach 1480 – 1580 nm, 1554 nm typical
OC-48:	Optical 1310 nm: Long Reach compliant Optical 1550 nm: Long Reach compliant Optional Dual 1310/1550 nm: Comprised of 1310 nm and 1550 nm laser options and additional 1 dB power reduction
STSX-1:	1.03 Vp ± 10%
Line Code	
OC-N	NRZ, Scrambled, N=1, 3, 3c, 12
STSX-1	B3ZS
Optical Frequency	
1310 nm	InGaAsP laser, RMS spectral width 4 nm max., Class 1 laser complies with 21 CFR 1040.10 and 1040.11
1550 nm	InGaAsP MQW DFB laser, spectral width 1 nm max. Class 1, complies with 21 CFR 1040.10 and 1040.11
Overhead Control and Monitoring	
Transmit control over bytes	Transport OH: A1, A2, C1, D1 through D12, E1, E2, F1, K1, K2 Z1, Z2 Path OH: C2, F2, G1, J1 (trace), Z3, Z4, Z5 VT OH: J2, Z6, Z7 (Byte Sync mode)
Receive Monitor	Transport OH: all bytes Path OH: all bytes VT OH: all bytes
Patterns	
STSX-1	Mapped DS1 (VT1.5 asynchronous and byte synchronous) M13, DS3, or STSX-1 drop/insert.
OC-N (N=1, 3, or 12)	Mapped DS1 (VT1.5 asynchronous and byte synchronous), M13, DS3, or STSX-1 drop/insert.
OC-3c	2^{23}-1 PRBS, 2^{23}-1 PRBS inverted (per 0.151), All 0's, All 1's.
OC-48	STS-3c/OC-3, STS-3c/OC-12, STS-12c/OC-12, STS-48c/OC-48, 2^{23}-1 PRBS (per 0.151), 2^{23}-1 PRBS inverted, 2^{23}-1 PRBS, All 0's, All 1's

SONET	Technical Specifications
Pointer Control	
STS	New value, single bursts, increment, decrement, increment-decrement, decrement-increment, T1X1 sequences, NDF control, SPE offset
VT	New Value, Single, increment, decrement, NDF control
SPE Frequency Offset	± 100 ppm
Results	Error Counts, Average Error Ratios, Current Error Ratios, Errored Seconds, Error Free Seconds, Alarm Seconds, and Event Counts.
Standards	ANSI, ITU, Bellcore, and AT&T specification including: OC-N: T1.105, G.703, G.772, G.957, G.958, 0.151, TR-NWT-000468TA-NWT-000983, GR-253-CORE STSX-1: T1.102, G.703, G.772, GR-253-CORE, GR-499-CORE, G.703
Switch Matrix Support	Allows the SONET test set to connect to the: DS1 line interface DS1 test set DS3 line interface DS3 test set M13 multiplex STSX-1 Drop/Insert ATM test set.
Test Results Storage	Test results can be saved to a file that can be viewed or printed at a later time.
Trouble Scan	Scans and displays all errors and alarms that have occurred during the current test.

DS1 Protocol Processor

The following shows the DS1 protocol processor technical specifications.

DS1	Technical Specifications
Alarm Detection	OOF, Pattern Sync, LOS, AIS, Yellow, COFA, excess 0's
Alarm Generation	AIS, Yellow, Idle
Automatic Configuration	Analyze incoming signal framing and line code and automatically configures the DS1 test set to match.
Clock	Internal, Received DS1 signal, Bits
Connectors	Dual Bantam

DS1	Technical Specifications
DS0 Access	
Transmit	Individual DS0 channels replaced with idle codes (0x7F) or AIS (0xFF)
Received	Monitor individual DS0 channel data, and signaling bits
DS0 Audible	Audible monitoring via u-law companding, G.711, G.712.
DS0 Signaling	AB (D4/SF), and ABCD (ESF) all channels at once.
Error Injection	BPV, pattern bit, Frame, CRC
Error Injection Rate	Single, 10^{-7} to 10^{-3}, User Programmable
Error Measurement	BPV, pattern bit, Frame, CRC
Framing	D4/SF, ESF, Unframed, SLC-96, unframed
Frequency	
Transmit	1.544 Mhz, ± 5ppm, -1 ppm/yr
Receive	1.544 Mhz, ± 200 ppm
History Graphs	Errors and alarms are graphed over a user selected time period. Each test set can independently log data for up to three days (72 hours).
Impedance	100 ohms, ±5% balanced
Input Jitter Tolerance	10 kHz - 100 kHz 0.4 UI 0dB line1 Hz 138 UI
Input Signal Measurement	Frequency Measurement Range: 1.544 Mhz, ± 200 ppm Peak positive and negative voltage range ± 0.1 Vp to ±7 Vp
Jitter Analyzer	Optional (ASA 312-05A), measures incoming line jitter.
Level Rx	
Monitor	100 ohms, 0 to -36 dBdsx with equalization; 16.532 to -19.468 dBm with equalization
Terminated	100 ohms, + 6 to -30 dBdsx with equalization; 22.532 to -13.468 dBm with equalization
Bridged	1000 ohms, 0 to -36 dBdsx with equalization; 16.532 to -19.468 dBm with equalization
Level Tx	DSX-1 (0 dBdsx ± 1dB) -7.5 dBdsx ± 1 dB cable simulation -15 dBdsx ± 1 dB cable simulation
Line Code	AMI, B8ZS
Loop Codes Support	
Transmit	In-band, Out-of-band, Line loopback, Payload loopback, 4-bit Smartjack, 5-bit Smartjack
Receive	Auto response on/off, Display of current loopback status

DS1	Technical Specifications
Patterns	QRSS, 2^{15}-1 PRBS, 2^{20}-1 PRBS, 2^{23}-1 PRBS (per 0.151), All 1's, All 0's, 1 in 8, 3 in 24, 1010, 24 Bit Programmable, Live Data, 55 DLY, T1-2, T1-3, T1-4, T1-5, 55 Octet, DDS-1, DDS-2, DDS-3, DDS-4, DDS-5, DDS-6, Bridge Tap, and Multi-Pattern. For Fractional T1 mode, the following patterns are available: 2^{6}-1 (63) PBRS, 2^{9}-1 (511) PRBS, 2^{11}-1 (2047) PRBS, and QRSS.
Results	Error Counts, Average Error Ratios, Current Error Ratios, Errored Seconds, Error Free Seconds, Alarm Seconds, and Event Counts.
Standards	ANSI, ITU, Bellcore and AT&T specifications including T1.403, T1. 408, G.703, G.772, O.151, GR-499-CORE, TR-TSY-000191, and Pub 62411.
Switch Matrix Support	Allows the DS1 test set to connect to the: DS1 line interface M13 multiplex SONET test set ATM test set (optional)
Test Results Storage	Test results can be saved to a file that can be viewed or printed at a later time.
Trouble Scan	Scans and displays all errors and alarms that have occurred during the current test.

DS3 Protocol Processor

The following shows the DS3 protocol processor technical specifications.

DS3	Technical Specification
Alarm Detection	OOF, Pattern Sync, LOS, AIS, Idle, Yellow/X-bit
Alarm Generation	AIS, Idle, Yellow/X-Bit
Clock	Internal
Connectors	BNC
Error Injection	BPV, pattern bit, Frame, P-Parity, C-Parity, FEBE
Error Injection Rate	Single, 10^{-7} to 10^{-3}, User Programmable
Error Measurement	BPV, pattern bit, Frame, P-Parity, C-Parity, FEBE
FEAC Codes	Alarm/Status codes, Loopback codes
Framing	M13, C-Bit Parity, Unframed
Frequency	44.736 Mhz, ± 12ppm (Tx), -2 ppm/yr 44.736 Mhz, ± 200ppm (Rx)

DS3	Technical Specification
History Graphs	Errors and alarms are graphed over a user selected time period. Each test set can independently log data for up to three days (72 hours).
Impedance	75 ohms, ± 5% unbalanced
Input Jitter Tolerance	10 Hz - 50 kHz, 20 UI > 50 kHz, UI reduce by 20 dB/decade
Input Signal Measurement	Frequency Measurement Range: 44.736 Mhz, ±200 ppm Peak positive and negative voltage range: ± 0.31 Vp to ±1.2 Vp
Jitter Analyzer	Optional (ASA 312-05A), measures incoming line jitter
Level Rx	
Terminated	75 ohms, + 6 to -12 dB relative to DSX3 with equalization.
Monitor	75 ohms, -15 to -26 dB relative to DSX3 with equalization.
Level Tx	
DS3 High	0.95 Vp ± 1.0 dB (0.847 Vp to 1.066 Vp)
DSX3	0.48 Vp ± 1.2 dB (0.418 Vp to 0.551 Vp)
DS3 Low	0.35 Vp ± 1.0 dB (0.312 Vp to 0.393 Vp)
Line Code	B3ZS
Patterns	2^{15}-1 PRBS, 2^{20}-1 PRBS, 2^{23}-1 PRBS (per 0.151), Idle (1100), Blue Signal (1010), All 1's, All 0's, User Defined (8 Bit Programmable), Live Data
Results	Error Counts, Average Error Ratios, Current Error Ratios, Errored Seconds, Error Free Seconds, Alarm Seconds, and Event Counts.
Standards	ANSI, ITU, Bellcore, and AT&T specification including T1.102, T1.404, T1.107, G.703, G.772, 0.151, TR-TSY-000009, TR-TSY-000191, GR-499-CORE, CB-119.
Switch Matrix Support	Allows the DS3 test set to connect to the: DS3 line interface SONET test set ATM test set (optional)
Test Results Storage	Test results can be saved to a file that can be viewed or printed at a later time.
Trouble Scan	Scans and displays all errors and alarms that have occurred during the current test.

ATM Protocol Processor

The following shows the ATM protocol processor technical specifications.

ATM	Technical Specifications
Adaptation Layers	AAL0, AAL1, and AAL5
Alarm Detection	Cell Synchronization Loss, AIS - F4 and F5 flow, RDI - F4 and F5 flow, PLCP Sync Seconds, PLCP Yellow Alarm, Selected Cells Not Received (SCNR) seconds, Status seconds, Loss of Pattern Sync seconds, PLCP Loss of Frame seconds, PLCP Out of Frame seconds
Alarm Generation	Cell Synchronization Loss, AIS - F4 and F5 flow (end-to-end/segment), RDI - F4 and F5 flow (end-to-end/segment), PLCP Yellow Alarm
ATM Management	Loopback cell
Channel Capacity Transmit	254 Channels
Receive	256 channels general analysis with 4 channels detailed analysis
Error Detection	Payload loss of pattern synchronization, AAL5 CRC errors, AAL5 length errors, PLCP Framing, LOF, OOF, AAL errors including SN & SNP errors, Loss of Cells, misinserted cells, BIT errors, PLCP FEBE, PLCP BIP, HEC errors
Error Generation	HEC Correctable, HEC Uncorrectable, BIT errors, PLCP BIP, PLCP FEBE, PLCP Framing (A1A2), PLCP Framing (POI)
Error Injection Rates	HEC correctable and uncorrectable errors with error rates from $1e^{-1}$ to $1e^{-9}$, error burst from 1 - 10, HEC errors single duration/continuous, VCC Payload bit error rate from $1e^{-1}$ to $1e^{-9}$.
Error Measurement	HEC error rate, HEC error count, HEC correctable and uncorrectable, payload PRBS errors.
History Graphs	Errors and alarms are graphed over a user selected time period. Each test set can independently log data for up to three days (72 hours).
Interface Support	UNI 3.1 and NNI
Line	STSX-1, OC-1, OC-3, OC12, DS1, DS3
Patterns	PRBS 2^{15}-1, All 1's, 10101010, User Defined pattern, Live
Permanent Virtual Circuit (PVC) Provisioning	Transmit: PDU cell count, Peak Cell Rate (PCR), Sustained Cell Rate (SCR), and Maximum Burst Size (MBS).

ATM	Technical Specifications
Physical Layers and Cell Mapping	STS-1, STS-3c, STS-12c, DS1 Direct, DS1 PLCP, DS3 Direct, DS3 PLCP
Quality of Service (QOS)	Cell transfer delay (min, max, mean), positive and negative cell delay variation (single point measurement; min, max, mean), cell loss count, cell loss ratio, cells received count, CRC errors count, length errors count
Results	Alarm seconds, error rates, errored seconds, error counts, error-free seconds
Standards	ANSI, ITU, and Bellcore specifications including GR-253-CORE, GR-820-CORE, GR-1248, TR-TSY-000009, TR-NWT-000253, I.356, I.363, I.610, O.151, T1.107-1988, T1.107a-1990, T1.231-1993, T1.511-1994, T1.629-1993.
Switch Matrix Support	Allows the ATM test set to connect to the: DS1 test set DS3 test set SONET test set
Test Results Storage	Test results can be saved to a file that can be viewed or printed
Traffic Management	Generic Cell Rate Algorithm (GCRA), Unspecified Bit Rate (UBR)
Trouble Scan	Scans and displays all errors and alarms that have occurred during the current test.
VP/VC Scan	Scan for active channels, scan for active channels with header mask

E1 Protocol Processor

The following shows the E1 protocol processor technical specifications.

E1	Technical Specifications
Alarm Detection	Loss of Pattern Sync, LOS, LOF, AIS, RAI, RMFAI, CASMFL
Alarm Generation	LOS, AIS, LOF, RAI (Yellow), RMFAI, CASMFL
Automatic Configuration	Analyze line coding, framing and pattern, and automatically configures the E1 test set to match.
Clock	Internal, Looped
Connectors	BNC
Error Injection	BPV, Bit, Frame, CRC, FEBE
Error Injection Rate	Single, 10^{-7} to 10^{-3}, User Programmable

E1	Technical Specifications
Error Measurement	BPV, Bit, Frame, CRC, FEBE
Framing	Unframed, PCM30, PCM30 CRC, PCM31, PCM31 CRC
Frequency	
Transmit	2.048 Mhz, ± 5 ppm
Receive	2.048 Mhz, ± 200 ppm
History Graphs	Errors and alarms are graphed over a user-selected time period. Each test set can independently log data for up to three days (72 hours).
Impedance	75 ohms, unbalanced
Level Rx	
Terminated	75 ohms, + 3 to -40 dBdsx with equalization
Level Tx	0 dBdsx ± 1dB (meets ITU G.703 pulse mask) -7.5 dBdsx ± 1 dB cable simulation -15 dBdsx ± 1 dB cable simulation
Line Code	AMI, HDB3 unbalanced
Loopback Mode	Line loopback
Patterns	2^6-1 PRBS, 2^6-1 PRBS INV, 2^9-1 PRBS, 2^9-1 PRBS INV, 2^11-1 PRBS, 2^11-1 PRBS INV, 2^15-1 PRBS, 2^15-1 PRBS INV, 2^20-1 PRBS, 2^20-1 PRBS INV, 2^23-1 PRBS, 2^23-1 PRBS INV, User Defined, 3-24 bit, Live (for Receive only)
Results	Error counts, error rates, error seconds, alarm seconds, errored seconds percentage, error free seconds percentage, alarm error rate, average and current error rate, and ITU G.823 analysis for bit, frame, CRC, and FEBE.
Standards	ITU including G.821, G.826, G.704, G.703.
Switch Matrix Support	Allows the E1 test set to connect to the: E1 line interface M13 Multiplexer to the DS3 line interface M13 Multiplexer to the SONET optical interface.
Trouble Scan	Scans and displays all errors and alarms that have occurred during the current test.