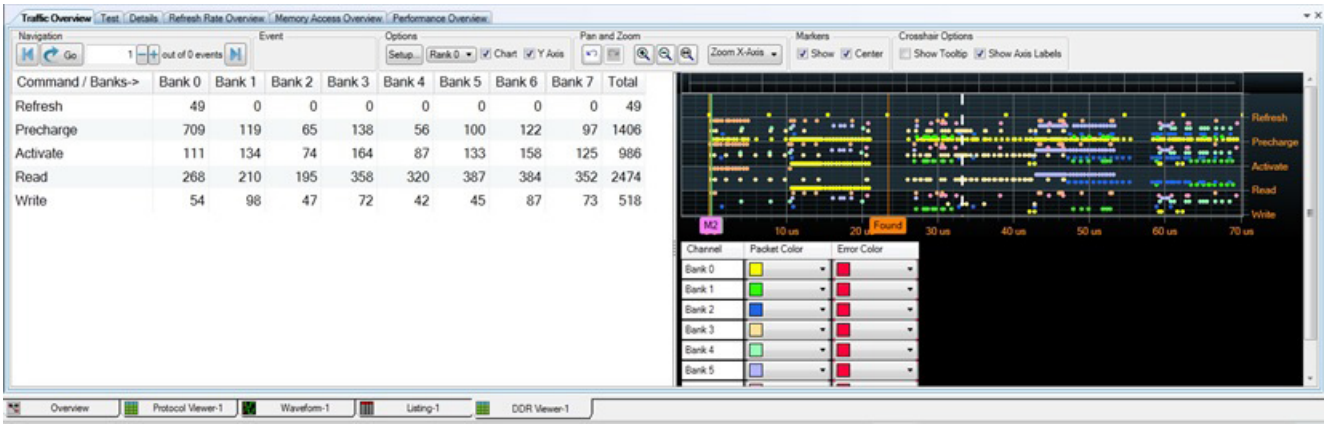
Keysight B4661A
Memory Analysis Software for Logic Analyzers

Data Sheet



KEYSIGHT TECHNOLOGIES

Unlocking Measurement Insights

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Overview

The Keysight B4661A memory analysis software offers a suite of tools that include the industry's first protocol compliance violation testing capability across speed changes, a condensed traffic overview for rapid navigation to areas of interest in the logic analyzer trace, powerful performance analysis graphics, and DDR and LPDDR decoders. With the B4661A memory analysis software and a Keysight logic analyzer [1], users can monitor DDR3/4 or LPDDR2/3/4 systems to debug, improve performance, and validate protocol compliance. Powerful traffic overviews, multiple viewing choices, and real-time compliance violation triggering help identify elusive DDR/LPDDR system violations.

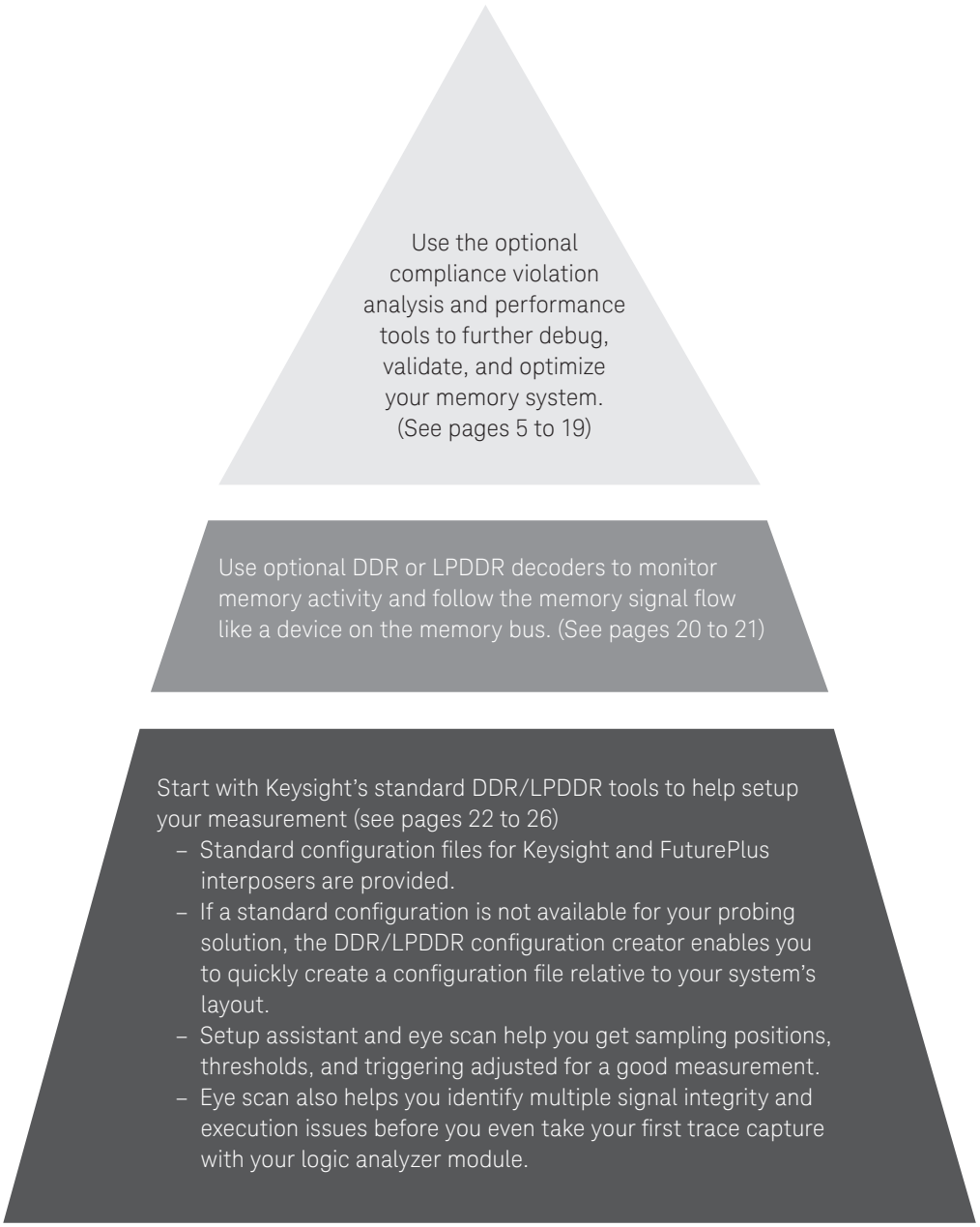
The Keysight B4661A memory analysis software provides four standard software features and four licensed memory analysis options.

Licensed software options
- DDR decoder with physical address trigger tool (B4661A-1xx)
- LPDDR decoder with physical address trigger tool for LPDDR/2/3 (B4661A-2xx)
- DDR and LPDDR compliance violation analysis toolset (B4661A-3xx)
  - Post-process compliance violation analysis
  - Real-time compliance violation analysis
- DDR3/4 and LPDDR2/3/4 performance analysis (B4661A-4xx)

Standard software features
- Default configurations for DDR and LPDDR probing solutions for Keysight logic analyzers [1]
- DDR setup assistant
- DDR eye finder/eye scan
- DDR configuration creator

1. B4661A is compatible with Keysight logic analyzers supported by Version 6.20 and higher of the logic and protocol analyzer software.

Overview (Continued)



DDR3/4 and LPDDR2/3/4 Performance Analysis Tool (B4661A-4FP/TP/NP)

Key features

- Traffic overview
  - Command graphing
  - Transaction decode
- Performance overview
  - Calculate and graph MByte data rates and % bus utilization
  - Address access mapping
    - By row and Col ADDR
    - By row ADDR and time
  - Refresh rate overview

Achieve greater insight faster using the B4661 memory analysis software for DDR3, DDR4, LPDDR2, LPDDR3, or LPDDR4. DDR/LPDDR memory measurement and debug work has become more complex and time consuming over the years as data rates increase and the architecture becomes more advanced. Using the DDR3/4 and LPDDR2/3/4 performance analysis tool, navigation to problem areas is simplified with a powerful new traffic overview that presents the logic analyzer trace capture at a high level with user-selected filtering.

Traffic Overview

Command graphing

Using traffic overview, each command on the bus is a row in the table. Columns vary depending on the viewing option chosen. Users choose from the following viewing options:

- View all ranks – in this mode, the table columns are “All ranks,” “Rank 0,” Rank 1,” etc. The chart shows a different color dot on a different line for each rank.
- View a single rank – The table columns are “All banks,” “Bank 0,” etc. (For DDR4, the columns are “All BG/BA”, then all combinations of BG and BA.) The chart shows one line of dots. A choice for which bank to view in the chart is enabled.
- All banks – The chart shows a dot for every command on the rank, regardless of bank. All dots are the same color.
- A single bank – The chart shows a dot for commands that apply only to the selected bank.
- If the user has a multi-rank system and wants to see charts of each rank simultaneously, then they can use multiple applications of the tool.

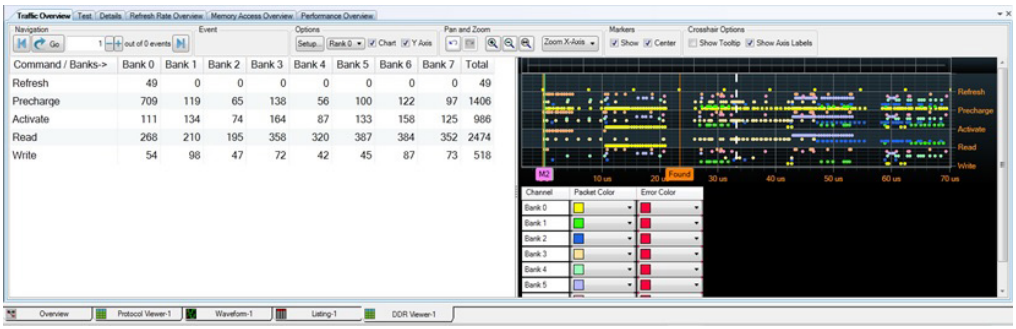


Figure 1. Traffic overview example: Graphing command activity by commands and banks across the captured trace from the Keysight logic analyzer.

The traffic overview containing transaction decode, summary calculations, meta-data, and graphing provides a condensed and insightful overview of system activity and enables powerful navigation to areas of interest.

DDR3/4 and LPDDR2/3/4 Performance Analysis Tool (B4661A-4FP/TP/NP) (Continued)

Transaction decode

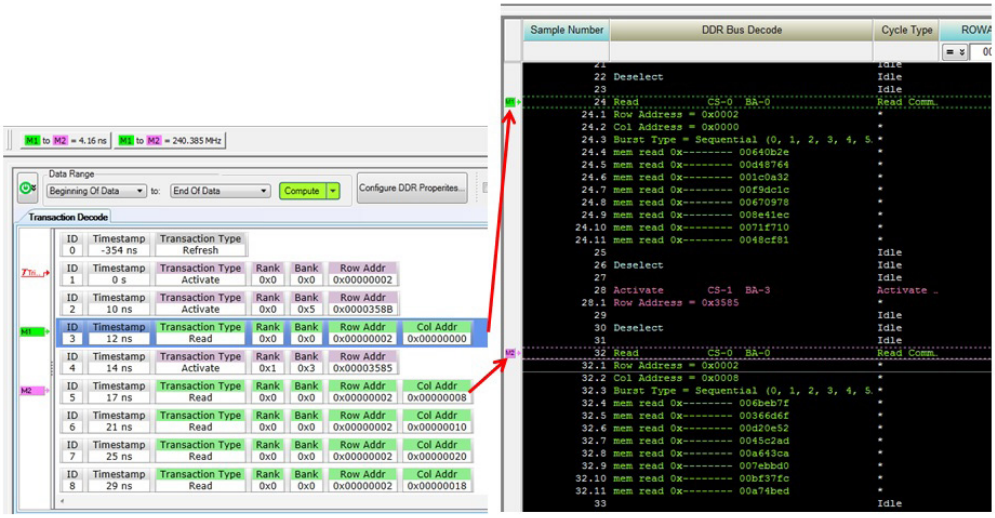


Figure 2. Transaction decode provides a high-level view that is time-correlated to the listing window where the more detailed DDR bus decoder results are viewed. (The transaction decode also includes a details window to see the data associated with each read or write transaction.)

Performance Overview

Calculate and graph MByte data rates and % utilization

Figure 3. Customize performance views by changing sample rate and performance measurement selections.

DDR3/4 and LPDDR2/3/4 Performance Analysis Tool (B4661A-4FP/TP/NP) (Continued)

Address access mapping

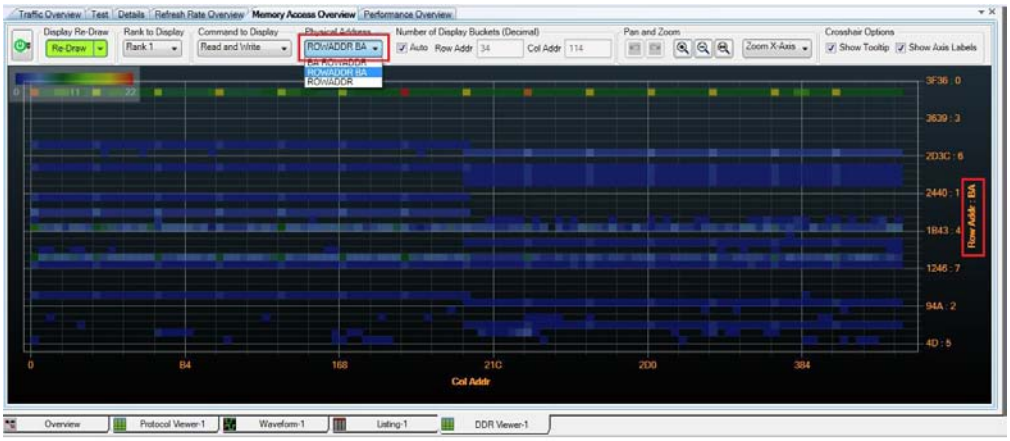


Figure 4. Address access heat map enables an overview of the number of accesses at specific row and col addresses.

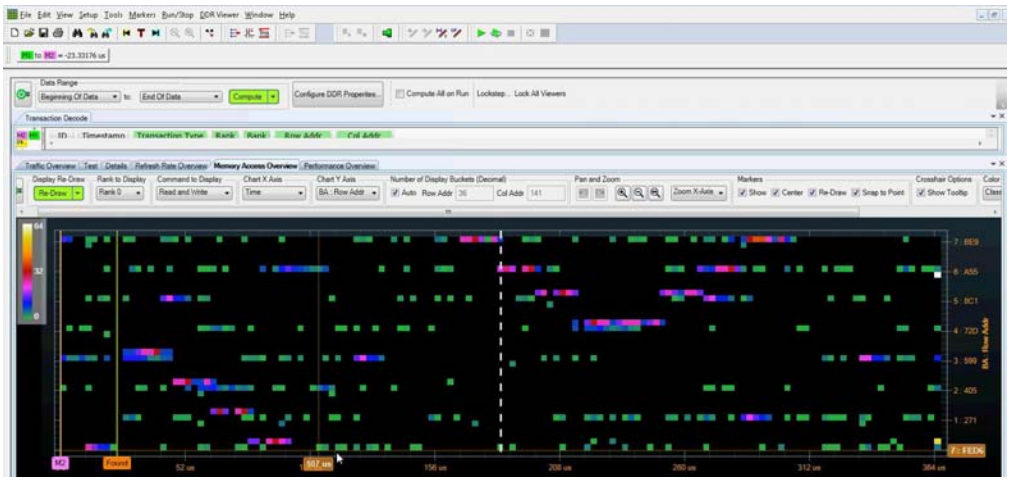


Figure 5. Users may also select row address and time as the axis on the address access heat map.

DDR3/4 and LPDDR2/3/4 Performance Analysis Tool (B4661A-4FP/TP/NP) (Continued)

Refresh rate overview

DDR/LPDDR memory is volatile. The charge on the memory cells (capacitors) needs to be "refreshed" to ensure memory values are retained. For DDR and LPDDR memory, there are two ways to refresh

- Issue the refresh command
- Issue a self-refresh command and put the memory into self-refresh mode for some length of time

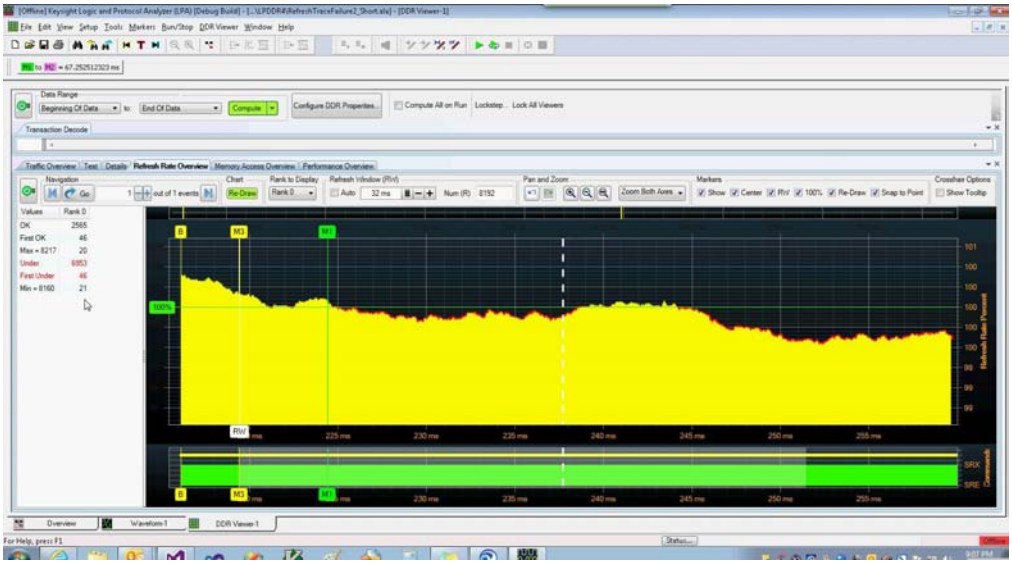


Figure 6. Refresh rate charts of LPDDR4 trace activity and quick pass/fail indication.

The refresh rate overview provides insight into refresh performance. It graphs refresh rate information for each sampled RW (refresh window) time window. By default, new refresh window samples are taken whenever there is a refresh event: refresh commands or entering/exiting self-refresh mode.

The X axis of this chart is time. The Y coordinate is the percent scale of expected refresh commands and self-refresh time found in the time window. The horizontal green line represents 100% for quick pass/fail indication. Red dots indicate areas that are under 100%.

Users can set the refresh window time (default 32 ms), the number (R) of refresh commands expected in the refresh window time, and the rank to display.

The highlighted box in the lower chart shows the refresh window time span for the sample at the "RW" marker point. The highlight box is red when under 100% and white when >= 100%.

DDR and LPDDR Compliance Violation Analysis Tool (B4661A-3FP/TP/NP)

The DDR and LPDDR compliance violation analysis toolset provides two tools under one license. Both compliance tools cover DDR, DDR2, DDR3, DDR4, LPDDR, LPDDR2, LPDDR3, and LPDDR4. The two tools are:

- Real-time compliance violation analysis
- Post-process violation analysis

Key features of both the post-process and real-time compliance violation tools:

- Test compliance violations across speed changes using the post-process compliance violation tool.
- Identify DDR/2/3/4 or LPDDR/2/3/4 state machine, protocol compliance, and protocol level bus cycle timing violations using either post-process or real-time tools.
- Save time with automated real-time DDR2/3/4 or LPDDR2/3/4 protocol compliance measurements and trace captures using the real-time compliance violation analysis tool.
- Edit parameters of the DDR/LPDDR standard preset tests easily using the enhanced parameter editing interface for both post-process and real-time tools.

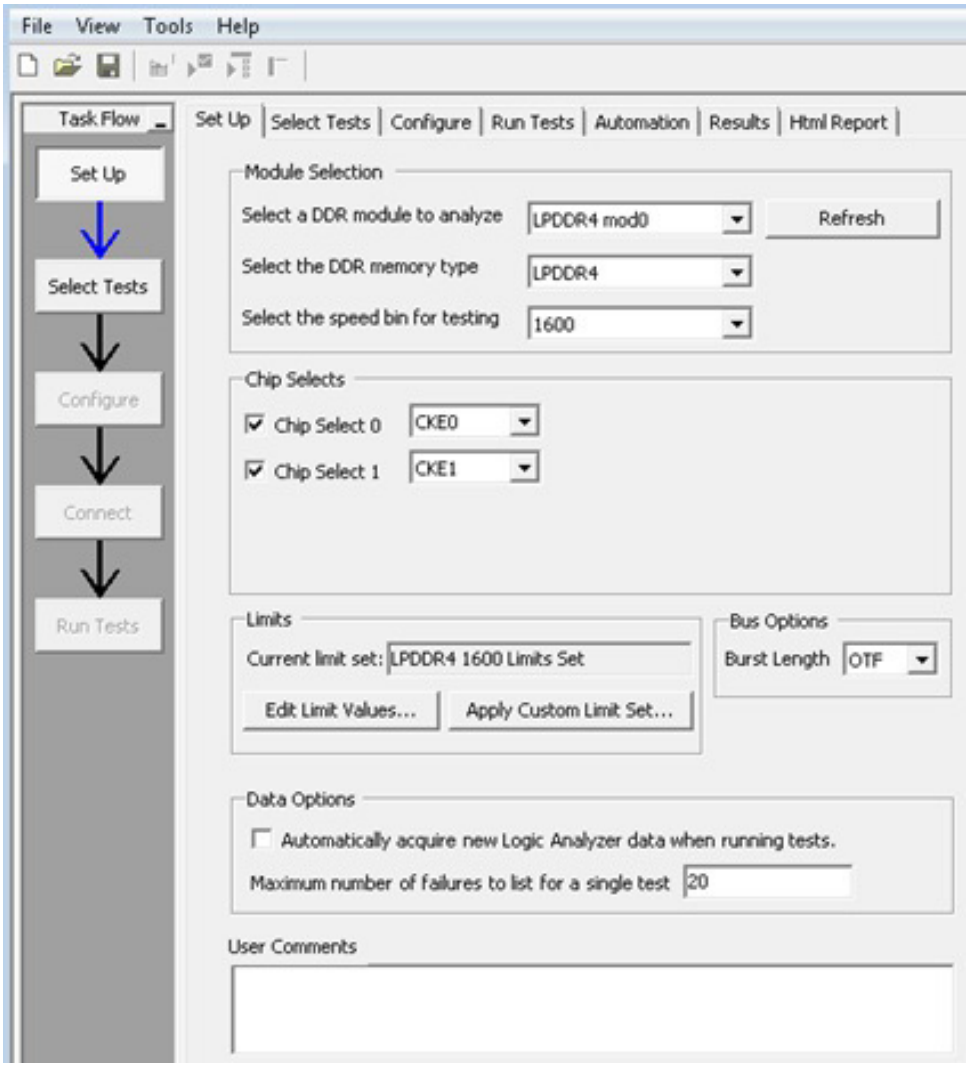


Figure 7. Both the real-time and post-process compliance tools provide user interfaces with pull-down selections to make setup easy.

Post-process and real-time compliance tools both contain dialogs with descriptions of the parameter values for ease of editing.

DDR and LPDDR Compliance Violation Analysis Tool (B4661A-3FP/TP/NP) (Continued)

Real-time compliance analysis

The automated real-time compliance analysis tool detects and captures state machine, protocol compliance, and protocol level bus cycle timing violations for DDR3/4 or LPDDR2/3/4. Real-time violation detection is an important advancement in DDR memory debug and validation. Monitoring your DDR bus real-time means the Keysight logic analyzer will continuously monitor the bus for the selected test and trigger if it occurs within the specified time frame. Beyond monitoring your DDR3/4 or LPDDR2/3/4 system real-time for elusive violations, designers can also monitor other digital system continuously for elusive, intermittent violations in protocol compliance or bus level timing.

Real-time testing enables

- Monitoring for compliance violations while running specific routines on the system under test.
- Unique feature of real-time compliance tool allows custom regression test suites to be created from a valid logic analyzer trigger for any valid Keysight logic analyzer configuration compatible with the B4661A.

The real-time compliance violation analysis tool cycles through preset or user-edited parameters for a selectable time limit on each parameter to capture logic analyzer traces of the complete ADD/CMD/DATA capture of the DDR/LPDDR bus triggering on the violation. The tool allows the user to save multiple traces of violations and produces a summary report when complete.

DDR and LPDDR Compliance Violation Analysis Tool (B4661A-3FP/TP/NP) (Continued)

Real-Time Violations

State machine violations common to DDR, DDR2, DDR3, DDR4 and LPDDR, LPDDR2, LPDDR3, LPDDR4	
READ or WRITE to an inactive row	
REFRESH to an active bank	
ACTIVATE to an active bank	
Real-time violations	
Compliance parameter	**Real-time compliance tests**
Parameters common to DDR, DDR2, DDR3, and LPDDR	
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRP	PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tCCD	WRITE to WRITE, READ to READ must be >= tCCD
tRFC	REFRESH to valid command (non_NOP/DESELECT) must be >= tRFC
tRRD	ACTIVATE to ACTIVATE (different banks) must be >= tRRD
tRC	ACTIVATE to ACTIVATE (same bank) must be >= tRC
tREFI	REFRESH to REFRESH <= tREFI*9
tMRD	MRS (Mode Register Set) to MRS must be >= tMRD
Additional DDR3 compliance parameters	
tZQoper	Long cal (normal operation) to valid command must be >= tZQoper
tZQCS	Short calibration (normal operation) to any valid command must be > tZQCS
tMOD	MRS (MODE Register Set) to valid command must be >= tMOD
tREFPDEN	REFRESH to power down entry >= tREFPDEN
tRDPDEN	READ to power down entry >= tRDPDEN
tWRPDEN	WRITE to power down entry >= tWRPDEN
tXPR	Exit RESET from CKE high to valid command >= tXPR
tXSDLL	Self refresh exit to valid command with DLL must be >= tXSDLL

DDR and LPDDR Compliance Violation Analysis Tool (B4661A-3FP/TP/NP) (Continued)

Real-Time Violations (Continued)

Compliance parameter	Real-time compliance tests
Additional DDR4 compliance parameters	
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRP	PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tDWR	WRITE to READ must be > tDWR
tCCD_L	WRITE to WRITE, same bank group must be >= tCCD_L
tRFC	REFRESH to valid command (non_NOP/DESELECT) must be >= tRFC
tRRD_L	ACTIVATE to ACTIVATE (same bank group) must be >= tRRD_L
tRC	ACTIVATE to ACTIVATE (same bank) must be >= tRC
tREFI	REFRESH to REFRESH <= tREFI*9
tZQoper	Long cal (normal operation) to valid command must be >= tZQoper
tZQCS	Short calibration (normal operation) to any valid command must be > tZQCS
tMRD	MRS (MODE Register Set) to MRS must be >= tMRD
tMOD	MRS (MODE Register Set) to valid command must be >= tMOD
tREFPDEN	REFRESH to power down entry >= tREFPDEN
tRDPDEN	READ to power down entry >= tRDPDEN
tWRPDEN	WRITE to power down entry >= tWRPDEN
tXPR	Exit RESET from CKE high to valid command >= tXPR
tXSDLL	Self refresh exit to valid command with DLL must be >= tXSDLL
tCKE	Duration of CKE high / low >= tCKE
Additional LPDDR2/3 compliance parameters	
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tDWR	WRITE to READ must be > tDWR
tCCD	WRITE to WRITE, must be >= tCCD
tRRD	ACTIVATE to ACTIVATE (different banks) must be >= tRRD
tZQCL	Long calibration command to any valid command (or CKE low) must be > tZQCL
tZQCS	Short calibration command to any valid command (or CKE low) must be > tZQCS
tZQINIT	Init calibration command to any valid command (or CKE low) must be > tZQINIT
tZQRESET	Reset calibration command to any valid command (or CKE low) must be > tZQRESET
tMRW	MRW command to any valid command (or CKE low) must be > tMRW
tMRR	MRR command to any valid command (or CKE low) must be > tMRR
tRFCab	REFRESH (all banks) to Active or Refresh must be > tRFCab
tRFCpb	REFRESH (per bank) to Activate (same bank) or REFRESH must be > tRFCpb
tRPab	PRECHARGE (all banks) to ACTIVE (any bank) must be >= tRPab
tRPpb	PRECHARGE (per bank) to ACTIVE (same bank) must be >= tRPpb
tCKE	Duration of CKE high / low >= tCKE
tXP	Exit Power down to any valid command >= tXP
tXSR	Exit self refresh to any valid command >=tXSR

DDR and LPDDR Compliance Violation Analysis Tool (B4661A-3FP/TP/NP) (Continued)

Real-Time Violations (Continued)

Compliance parameter	Real-time compliance tests
Additional LPDDR4 compliance parameters	
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRTP	READ to PRECHARGE must be >= tRTP
tCCD	READ -1 or any write (any bank) to READ-1 or any write (any bank) must be >= tCCD
tCCDMW	Any write to MASKED WRITE (same bank) must be > =tCCDMW
tRRD	ACTIVATE-2 to ACTIVATE-2 (different banks) must be >=tRRD
tMRW	MRW-2 to any valid command must be >= tMRW
tMRR	MRR-1 to any valid command must be >= tMRR
tRPab	PRECHARGE (all banks) to ACTIVATE-2/REFRESH (any bank) >= tRPab
tRPpb	PRECHARGE (per bank) to ACTIVATE-2 (same bank) or REFRESH (same bank or all banks) must be >= tRPpb
tXSR	Exit self refresh to any valid command >= tXSR
tPPD	Precharge (any bank to Precharge (any bank) must be >= tPPD
tRFCab	REFRESH (all banks to ACTIVATE-2 or REFRESH >= tRFCab
tRFCpd	REFRESH (per bank) to ACTIVATE-2 (same bank) or REFRESH > tRFCpb
tREFI	REFRESH command to REFRESH command must be <=tREFI*9
tCKE	Duration of CKE high / low >= tCKE
tESCKE	Self Refresh Entry command to CKE low must be >= tESCKE
tCMDCKE	Any valid command to CKE low must be >= tCMDCKE
tCKEHCMD	Exit powerdown to any valid command >= tCKEHCMD
tMMRRIa	Exit powerdown to MRR >= tMRRIa (where tMRRIa = tXP (tCKEHCMD) + tMRRI)
BL16	Write/Read/Precharge - BL16 - Select these tests if your system uses fixed BL16
BL32	Write/Read/Precharge - BL16 - Select these tests if your system uses fixed BL32
BL OTF	Write/Read/Precharge - BL16 - Select these tests if your system uses Burst length OTF (on the fly)
MWtoP	MASKED WRITE-1 to PRECHARGE (same bank) >= MWtoP
MWtoR	MASKED WRITE-1 to READ (same bank) >= MWtoR
RFtoLAT	RD_FIFO to ZQCALLATCH >= RFtoLAT
RFtoLAT	RD_CALIBRATION to ZQCALLATCH >= RFtoLAT
RFtoLAT	MRR to ZQCALLATCH >= RFtoLAT
WFtoLAT	WR_FIFO to ZQCALLATCH >= WFtoLAT
WFtoLAT	MASKED WRITE-1 to ZQCALLATCH >= WFtoLAT
tZQCAL	ZQCALSTART to ZQCALLTACH >= tZQCAL
tZQLAT	ZQCALLATCH to any valid command >= tZQLAT
tZQRESET	ZQCALRESET to any valid COMMAnd >= tZQRESET

DDR and LPDDR Compliance Violation Analysis Tool (B4661A-3FP/TP/NP) (Continued)

Post-process compliance violation analysis tool

The post-process compliance violation analysis tool automates state machine, protocol compliance, and protocol level bus cycle timing violation detection across Keysight logic analyzer traces. HTML reports of test results show margin details for both passing and failing tests.

Use the post-process compliance application tool to:

- Spot check logic analyzer traces for violations.
- Check logic analyzer trace captures leading up to system crashes for possible violations before the crash.

Post-process testing enables:

- Compliance violation testing across speed changes.
- “Click to” and “mark violation” features to quickly navigate from the compliance tool to violations in the traffic overview graph, waveform, or listing window.
- Margin information on each parameter to understand the range relative to the specification.

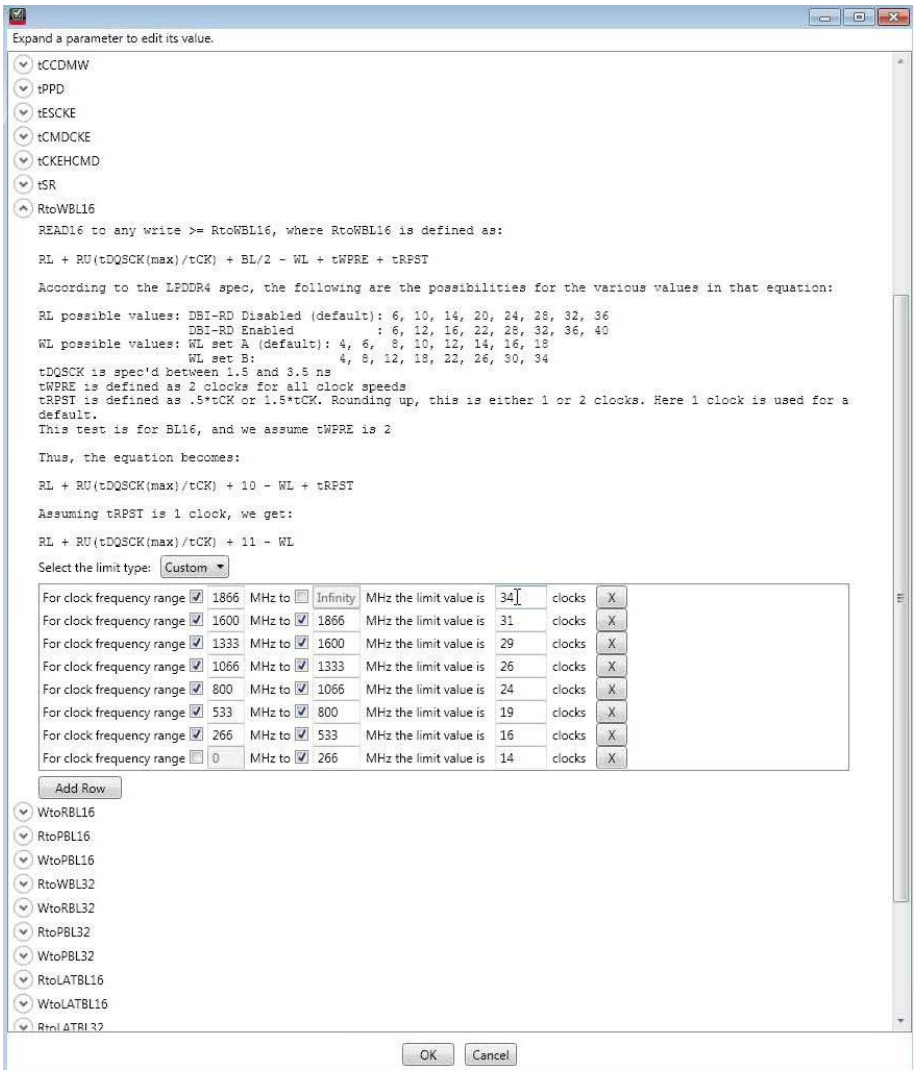


Figure 8. Speed ranges can be added in the post-process compliance tool for any parameter that has different criteria based on speed.

DDR and LPDDR Compliance Violation Analysis Tool (B4661A-3FP/TP/NP) (Continued)

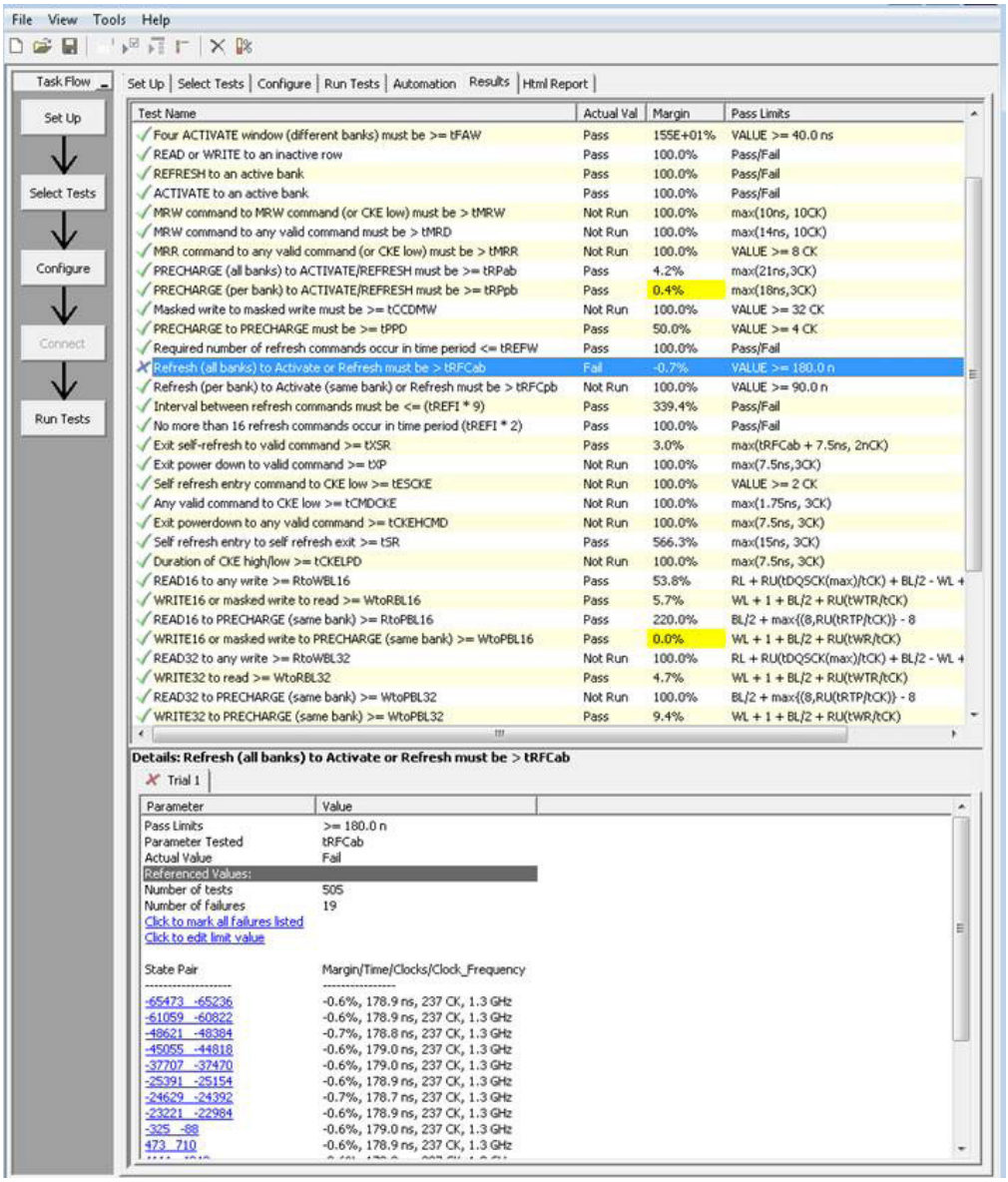


Figure 9. The post-process compliance tool includes hyperlinks to jump quickly to and/or mark violations and worst-case violations in the logic analyzer traces, transaction overview, and listing windows.

DDR and LPDDR Compliance Violation Analysis Tool (B4661A-3FP/TP/NP) (Continued)

Post Process Compliance Tests

State machine violations common to DDR, DDR2, DDR3, DDR4 and LPDDR, LPDDR2, LPDDR3, LPDDR4	
READ to WRITE to an inactive row	
REFRESH to an active bank	
ACTIVATE to an active bank	
Post-process violations	
Compliance parameter	**Post-process compliance tests**
Parameters common to DDR, DDR2, DDR3, and LPDDR	
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRP	PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tDWR	WRITE to READ must be > tDWR
tCCD	WRITE to WRITE, READ to READ must be >= tCCD
tRFC	REFRESH to valid command (non_NOP/DESELECT) must be >= tRFC
tRRD	ACTIVATE to ACTIVATE (different banks) must be >= tRRD
tFAW	Four ACTIVATE window (different banks) must be>= tFAW
tRC	ACTIVATE to ACTIVATE (same bank) must be >= tRC
tREFI	REFRESH to REFRESH <= tREFI*9
tMRD	MRS (Mode Register Set) to MRS must be >= tMRD
Additional DDR3 compliance parameters	
tZQoper	Long cal (normal operation) to valid command must be >= tZQoper
tZQCS	Short calibration (normal operation) to any valid command must be > tZQCS
tMOD	MRS (MODE Register Set) to valid command must be >= tMOD
tREFPDEN	REFRESH to power down entry >= tREFPDEN
tRDPDEN	READ to power down entry >= tRDPDEN
tWRPDEN	WRITE to power down entry >= tWRPDEN
tXPR	Exit RESET from CKE high to valid command >= tXPR
tXSDLL	Self refresh exit to valid command with DLL must be >= tXSDLL
tXPDLL	Exit precharge power down with DLL to any valid command < tXPDLL
Additional DDR4 compliance parameters	
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRP	PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tDWR	WRITE to READ must be > tDWR
tCCD_L	WRITE to WRITE, same bank group must be >= tCCD_L
tRFC	REFRESH to valid command (non_NOP/DESELECT) must be >= tRFC
tFAW	Four ACTIVATE window (different banks) must be>= tFAW
tRRD_L	ACTIVATE to ACTIVATE (same bank group) must be >= tRRD_L
tRC	ACTIVATE to ACTIVATE (same bank) must be >= tRC
tREFI	REFRESH to REFRESH <= tREFI*9

DDR and LPDDR Compliance Violation Analysis Tool (B4661A-3FP/TP/NP) (Continued)

Post Process Compliance Tests (Continued)

Compliance parameter	Post-process compliance tests
Additional DDR4 compliance parameters (Continued)	
tZQoper	Long cal (normal operation) to valid command must be >= tZQoper
tZQCS	Short calibration (normal operation) to any valid command must be > tZQCS
tMRD	MRS (MODE Register Set) to MRS must be >= tMRD
tMOD	MRS (MODE Register Set) to valid command must be >= tMOD
tREFPDEN	REFRESH to power down entry >= tREFPDEN
tRDPDEN	READ to power down entry >= tRDPDEN
tWRPDEN	WRITE to power down entry >= tWRPDEN
tXPR	Exit RESET from CKE high to valid command >= tXPR
tXSDLL	Self refresh exit to valid command with DLL must be >= tXSDLL
tXPDLL	Exit precharge power down with DLL to any valid command < tXPDLL
Additional LPDDR2/3 compliance parameters	
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tDWR	WRITE to READ must be > tDWR
tCCD	WRITE to WRITE, must be >= tCCD
tRRD	ACTIVATE to ACTIVATE (different banks) must be >= tRRD
tFAW	Four ACTIVATE window (different banks) must be>= tFAW
tZQCL	Long calibration command to any valid command (or CKE low) must be > tZQCL
tZQCS	Short calibration command to any valid command (or CKE low) must be > tZQCS
tZQINIT	Init calibration command to any valid command (or CKE low) must be > tZQINIT
tZQRESET	Reset calibration command to any valid command (or CKE low) must be > tZQRESET
tMRW	MRW command to any valid command (or CKE low) must be > tMRW
tMRR	MRR command to any valid command (or CKE low) must be > tMRR
tREFBW	Greater than 8 REFRESH all bank commands in tREFBW
tREFW	Required number of refresh commands occur in time perion <= tREFW
tRFCab	REFRESH (all banks) to Active or Refresh must be > tRFCab
tRFCpb	REFRESH (per bank) to Activate (same bank) or REFRESH must be > tRFCpb
tRPab	PRECHARGE (all banks) to ACTIVE (any bank) must be >= tRPab
tRPpb	PRECHARGE (per bank) to ACTIVE (same bank) must be >= tRPpb
tCKE	Duration of CKE high / low >= tCKE
tXP	Exit Power down to any valid command >= tXP
tCKESR	Duration of self-refresh >= tCKESR
tDPD	Duration of power down to valid command >= tDPD
tXSR	Exit self-refresh to valid command >= tXSR
tXSR	Exit self refresh to any valid command >=tXSR

DDR and LPDDR Compliance Violation Analysis Tool (B4661A-3FP/TP/NP) (Continued)

Post Process Compliance Tests (Continued)

Compliance parameter	Post-process compliance tests
LPDDR4	
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tCCD	READ -1 or any write (any bank) to READ-1 or any write (any bank) must be >= tCCD
tCCDMW	Any write to MASKED WRITE (same bank) must be >= tCCDMW
tRRD	ACTIVATE-2 to ACTIVATE-2 (different banks) must be >= tRRD
tMRW	MRW-2 to any valid command must be >= tMRW
tMRR	MRR-1 to any valid command must be >= tMRR
tRPab	PRECHARGE (all banks) to ACTIVATE-2/REFRESH (any bank) >= tRPab
tRPpb	PRECHARGE (per bank) to ACTIVATE-2 (same bank) or REFRESH (same bank or all banks) must be >= tRPpb
tXSR	Exit self refresh to any valid command >= tXSR
tPPD	Precharge (any bank to Precharge (any bank) must be >= tPPD
tRFCab	REFRESH (all banks to ACTIVATE-2 or REFRESH >= tRFCab
tRFCpd	REFRESH (per bank) to ACTIVATE-2 (same bank) or REFRESH > tRFCpb
tCKE	Duration of CKE high/low >= tCKE
tESCKE	Self Refresh Entry command to CKE low must be >= tESCKE
tCMDCKE	Any valid command to CKE low must be >= tCMDCKE
tCKEHCMD	Exit powerdown to any valid command >= tCKEHCMD
tSR	Self refresh entry to self refresh exit >= tSR
tMMRRIa	Exit powerdown to MRR >= tMRRIa (where tMRRIa = tXP (tCKEHCMD) + tMRRI)
BL16	Write/Read/Precharge - BL16 - Select these tests if your system uses fixed BL16
BL32	Write/Read/Precharge - BL16 - Select these tests if your system uses fixed BL32
BL OTF	Write/Read/Precharge - BL16 - Select these tests if your system uses Burst length OTF (on the fly)
MWtoP	MASKED WRITE-1 to PRECHARGE (same bank) >= MWtoP
MWtoR	MASKED WRITE-1 to READ (same bank) >= MWtoR
RFtoLAT	RD_FIFO to ZQCALLATCH >= RFtoLAT
RFtoLAT	RD_CALIBRATION to ZQCALLATCH >= RFtoLAT
RFtoLAT	MRR to ZQCALLATCH >= RFtoLAT
WFtoLAT	WR_FIFO to ZQCALLATCH >= WFtoLAT
WFtoLAT	MASKED WRITE-1 to ZQCALLATCH >= WFtoLAT
tZQCAL	ZQCALSTART to ZQCALLTACH >= tZQCAL
tZQLAT	ZQCALLATCH to any valid command >= tZQLAT
tZQRESET	ZQCALRESET to any valid COMMAnd >= tZQRESET

DDR and LPDDR Compliance Violation Analysis Tool (B4661A-3FP/TP/NP) (Continued)

Post Process Compliance Tests (Continued)

Compliance parameter	Post process / Compliance tests
LPDDR4	**Refresh tests**
tREFI*9	REFRESH command to REFRESH command must be <=tREFI*9
tREFW	Required number of refresh commands occur in time period <= tREFW
tRFCab	Refresh (all banks) to Activate or Refresh must be > tRFCab
tRFCpb	Refresh (per bank) to Activate (same bank) or Refresh must be > tRFCpb
tREFI*2	No more than 16 refresh commands occur in time period (tREFI *2)
LPDDR4	**Power down and self-refresh tests**
tXSR	Exit Self-Refresh to valid command >= tXSR
tXP	Exit power down to valid command >= tXP
tESCKE	Self-Refresh entry command to CKE low >= tESCKE
tCMDCKE	Any valid command to CKE low >= tCMDCKE
tCKEHCMD	Exit powerdown to any valid command >= tCKEHCMD
tSR	Self refresh entry to self refresh exit >= tSR
tMRRIa	Exit powerdown to MRR >= tMRRIa (tXP + tMRRI)
tCKE	Duration of CKE high/ low >= tCKE
LPDDR4	**Write/Read/Precharge/Cal - BL16 - Select these tests if your system uses fixed BL 16**
RtoWBL16	READ16 to any write >= RtoWBL16
WtoRBL16	WRITE16 to READ16 >= WtoRBL16
RtoRBL16	READ16 to PRECHARGE (same bank) >= RtoRBL16
WtoPBL16	WRITE16 to PRECHARGE (same bank) >= WtoPBL16
RtoLATBL16	READ32 to ZQCALLATCH >= RtoLATBL16
WtoLATBL16	WRITE32 to ZQCALLATCH >= WtoLATBL16
LPDDR4	**Write/Read/Precharge/Cal - BL32 - Select these tests if your system uses fixed BL 32**
RtoWBL32	READ32 to any write >= RtoWBL32
WtoRBL32	WRITE32 to READ16 >= WtoRBL32
RtoRBL32	READ32 to PRECHARGE (same bank) >= RtoRBL32
WtoPBL32	WRITE32 to PRECHARGE (same bank) >= WtoPBL32
RtoLATBL32	READ32 to ZQCALLATCH >= RtoLATBL32
WtoLATBL32	WRITE32 to ZQCALLATCH >= WtoLATBL32
LPDDR4	**Write/Read/Precharge/Cal - BL OTF - Select these tests if your system uses fixed BL OTF (on the fly)**
RtoWBL16OTF	READ32 to any write >= RtoWBL16OTF
WtoRBL16OTF	WRITE32 to READ16 >= WtoRBL16OTF
RtoRBL16OTF	READ32 to PRECHARGE (same bank) >= RtoRBL16OTF
WtoPBL16OTF	WRITE32 to PRECHARGE (same bank) >= WtoPBL16OTF
RtoWBL32otf	READ32 to any write >= RtoWBL32OTF
WtoRBL32OTF	WRITE32 to READ16 >= WtoRBL32OTF
RtoRBL32OTF	READ32 to PRECHARGE (same bank) >= RtoRBL32OTF
WtoPBL32OTF	WRITE32 to PRECHARGE (same bank) >= WtoPBL32OTF
RtoLATBL16OTF	READ32 to ZQCALLATCH >= RtoLATBL32OTF
WtoLATBL16OTF	WRITE32 to ZQCALLATCH >= WtoLATBL32OTF
RtoLATBL32OTF	READ32 to ZQCALLATCH >= RtoLATBL32OTF
WtoLATBL32OTF	WRITE32 to ZQCALLATCH >= WtoLATBL32OTF

DDR Decoder with Physical Address Trigger Tool (B4661A-1FP/TP/NP)

The B4661A DDR decoder covers DDR/2/3/4 and provides protocol decoding of memory transactions on traces captured using a Keysight logic analyzer. The protocol decoding software translates acquired signals into easily-understood colorized bus transactions showing associated data bursts for double-edge data rate captures.

Key features

- Decodes DDR, DDR2, DDR3 and DDR4 commands and MRS commands
  - Includes selection to decode MRS of DDR4 RDIMM and LRDIMM.
- Enables fast physical address trigger setup with physical address trigger tool.

Figure 10. DDR decoder display in listing window.

LPDDR Decoder (B4661A-2FP/TP/NP)

Key features

- Decodes LPDDR, LPDDR2, LPDDR3 and LPDDR4 commands and MRS commands
- Enables fast physical address trigger setup for LPDDR2/3

Using the LPDDR decoder, valid read and write commands are decoded to include row and column addresses and the complete data burst associated with the command.

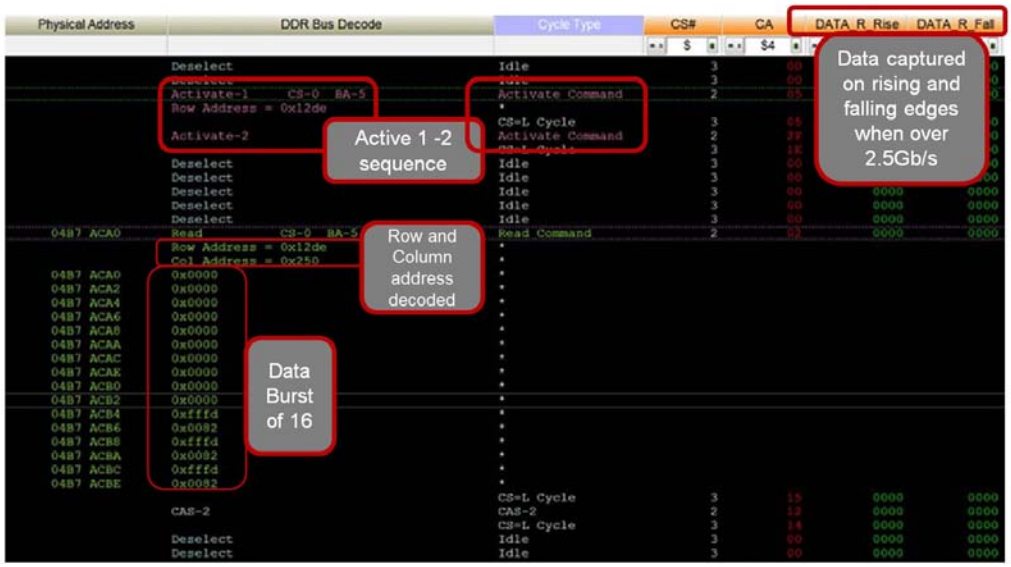


Figure 11. LPDDR4 decode in listing window.

Physical address conversion tool in both DDR3/4 and LPDDR2/3 decoders with integrated trigger creation

Setting up a trigger on a specific physical address to obtain the corresponding data bus can be very tedious. The physical address trigger tool is included in the B4661A DDR decoder and LPDDR decoder options. The trigger tool allows you to automatically create a trigger on a specific physical address without having to go through a step-by-step trigger add-in. The physical address trigger tool incorporates a user-friendly interface to help the user quickly setup the trigger. DDR2/3/4 and LPDDR2/3 are covered by the physical address trigger tool. LPDDR4 is not covered by the physical address trigger tool.

B4661A Standard Software Features

Standard Software Tools

B4661A standard software features for DDR/LPDDR memory compliance testing and debug

- Default DDR probing configurations
- DDR setup assistant
- DDR eye finder/eye scan
- DDR configuration creator

Default DDR Probing Configurations

Default configurations for Keysight DDR and LPDDR memory probes are available at no charge as part of the Keysight B4661A memory analysis software package. Default configurations include all labels and settings required to interface with the DDR setup assistant tool for rapid tuning of state mode measurements. Keysight default configurations include:

- Labeling and grouping of signals appropriate for each memory probe
- Symbol tables for command labels
- Trigger favorites for memory applications:
  - Basic trigger (simple read/write trigger)
  - Mode register settings (trigger to display mode register settings)
  - Filter NOPs (trigger to filter some of the NOPs)
  - Burst 4 write data (trigger to occur on a unique 4 burst write)
  - Burst 8 write data (trigger to occur on a unique 8 burst write)

DDR Setup Assistant

DDR measurements made fast, easy, and powerful

The DDR setup assistant simplifies measurement setup and minimizes the time to tune state mode measurements on the logic analyzer. DDR setup assistant guides you through even the most complex logic analyzer setup in minutes. It includes a variety of powerful, time-saving trigger features optimized for DDR measurements. The tool automatically configures optimum thresholds and controls DDR eye finder scans to rapidly locate optimal sample positions.

The DDR setup assistant tool is available at no charge as part of the Keysight B4661A memory analysis software package.

B4661A Standard Software Features (Continued)

DDR Eye Finder/Eye Scan

DDR eye scan makes it easy to determine the optimum acquisition sample point without requiring an oscilloscope. Qualified scans place the sample position at the center of the eye on every individual channel for maximum data capture reliability, including separate sampling positions for read and write data. Interface selections allow the user to customize scans for particular views and conditions of interest.

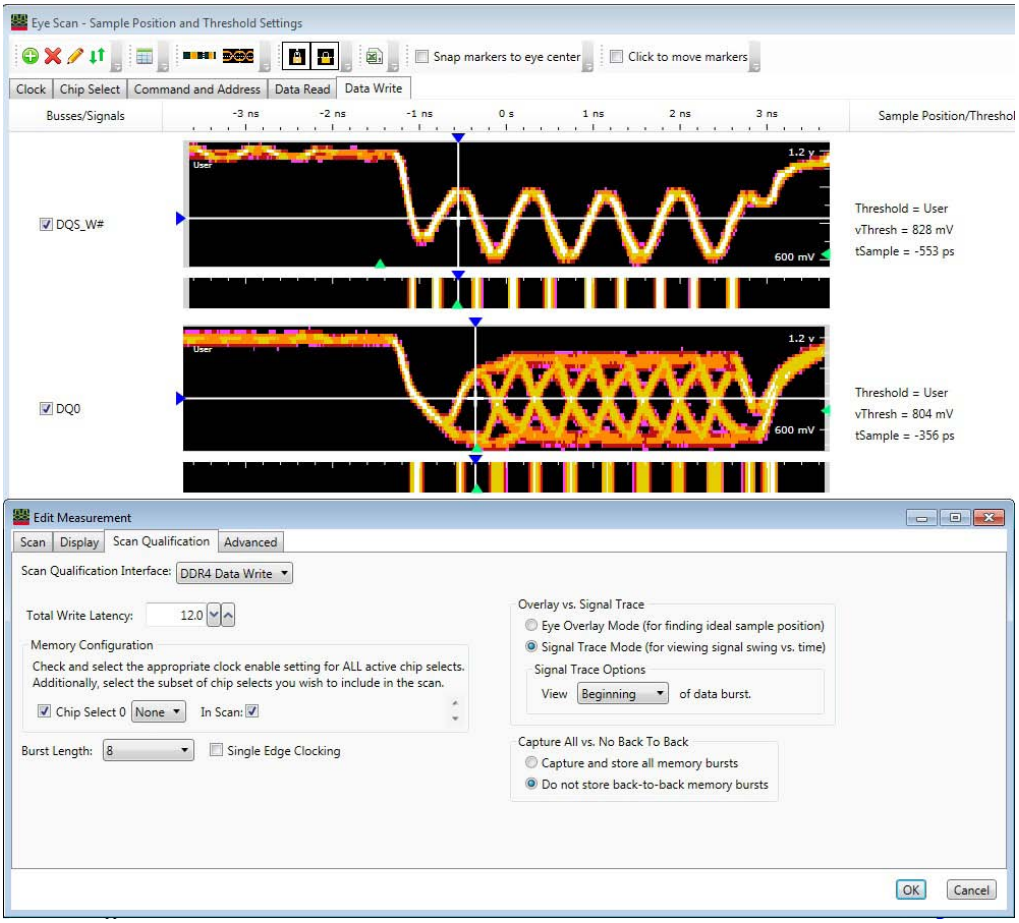


Figure 12. The DDR eye scan interface provides easy-to-follow pull-downs and options that control powerful scan qualifications for the user. Burst qualified eye scans from signal trace mode allow you to view the activity on the signals only when a burst is taking place. Screen shot above shows DDR4 2400 Mb/s read DQS and read DQ0 scanned in signal trace mode with no back-to-back bursts.

Increased insight decreases test time. Eye scan helps you identify bus level signal integrity and execution issues before you even take your first measurement by providing qualitative comparisons of eye diagrams relative to each other that allow you to quickly identify abnormalities at a glance.

Bus-level SI insight is the ability to view eye scans of up to hundreds of signals in a bus relative to each other. It is important because it provides:

- Quick, qualitative comparisons
  - Between signals in scan
  - Between scans where one variable has changed
  - More signals than possible on scope
- Powerful scan qualification provides views not easily obtained by any other method

B4661A Standard Software Features (Continued)

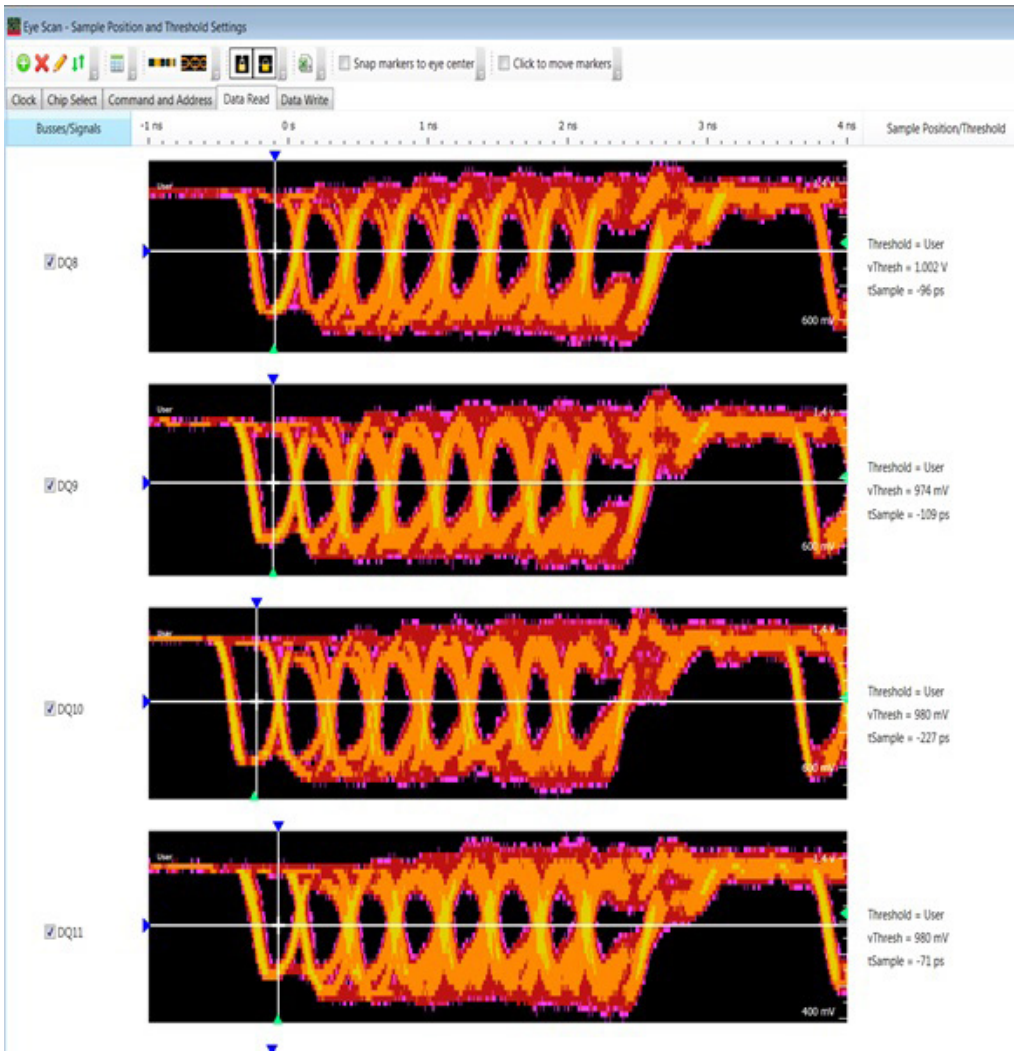


Figure 13. In this DDR4 at 3.1 Gb/s eye scan screen shot, scanned as read bursts with no back-to back transactions, using signal trace mode in DDR eye scan, we can quickly see that the first sample in the burst does not drive to the lowest value within the time of the first data sample. This indicates the possibility of Inter-Symbol Interference from either insufficient DRAM drive strength or incorrect termination settings.

B4661A Standard Software Features (Continued)

DDR Configuration Creator

The DDR/LPDDR configuration creator tool allows you to define the footprints layout per your custom probing solution used in the DDR/LPDDR setup and then create an XML configuration file based on your footprint information with the click of a button. The generated XML configuration file contains all the information for your custom probing required for the Keysight B4661A memory analysis software tools.

Once your custom XML configuration is created, it can be selected by the Keysight DDR setup assistant tool to define the DDR/LPDDR acquisition setup for your Keysight logic analyzer. By using a custom configuration file, you can ensure that the logic analyzer setup is correctly and completely set for a custom probing scenario.

The DDR configuration creator tool enables

- Naming of footprints from schematic drawings.
- Tracking and highlighting which signals have already been assigned, helping to ensure that the user doesn't miss a signal or incorrectly double-assign a signal.
- Selection of either Soft Touch Pro footprints (three different schematic views) or custom (per pod) for signal assignments.

Supported bus types

The DDR configuration creator tool can generate configuration files for the following DDR/LPDDR bus types.

- DDR3
- DDR4 (< 2.5 GHz and > 2.5 GHz clock rates)
- LPDDR2
- LPDDR3
- LPDDR4 (< 2.5 GHz and > 2.5 GHz clock rates)

B4661A Standard Software Features (Continued)

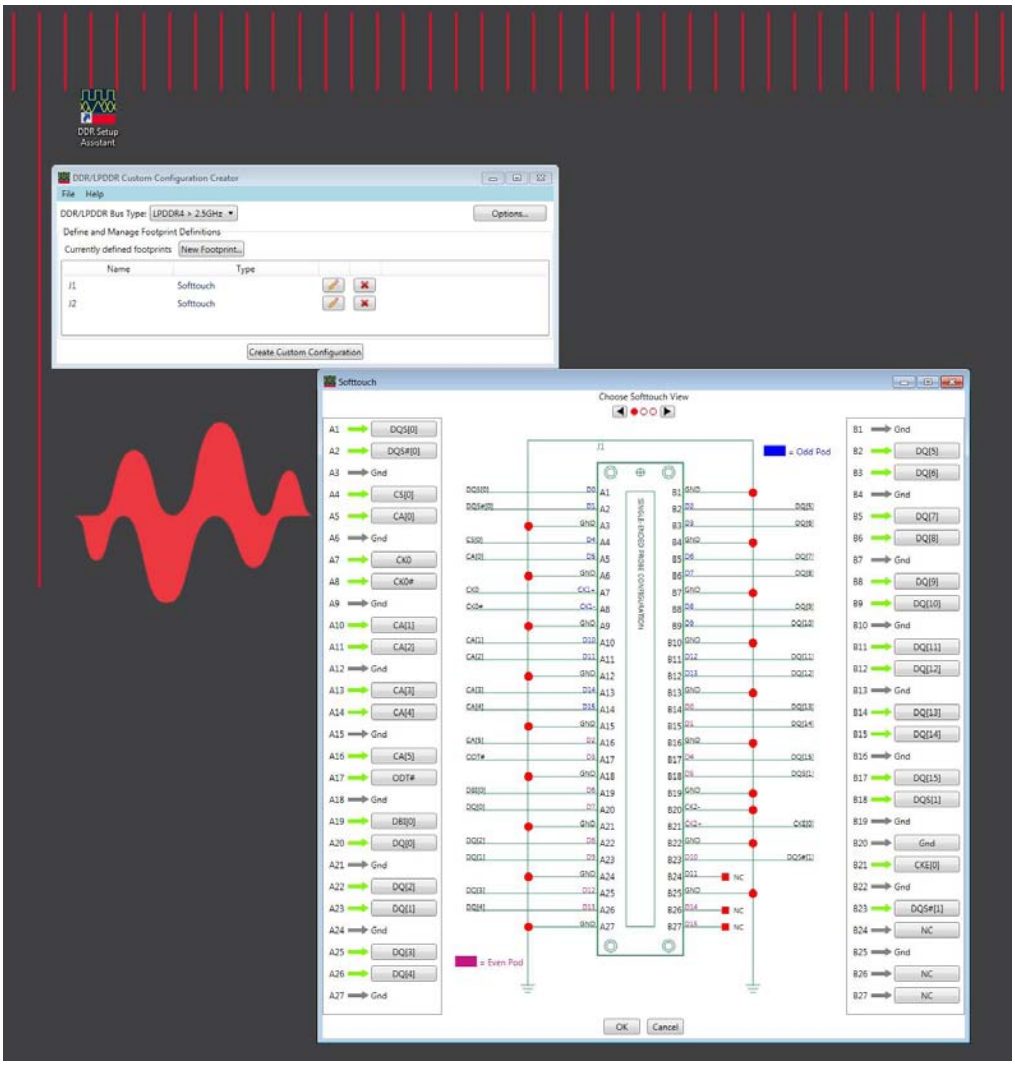


Figure 14. The DDR configuration creator tool lets you define Soft Touch Pro footprint or custom (per logic analyzer Pod) pin assignments.

B4661A Memory Analysis Software Characteristics

Logic Analyzer Compatibility

The B4661A memory analysis software is compatible with the following logic analyzer modules:

Product	Description
U4154B	136-channel, 4 Gb/s state, AXIe-based logic analyzer module with ability to merge up to three modules
U4154A	136-channel, 4 Gb/s state, AXIe-based logic analyzer module with ability to merge up to two modules
16850 Series	Portable logic analyzers

Required Software

- Logic and protocol analyzer software, version 6.20 or higher
- B4661A memory analysis software

B4661A Memory Analysis Software Includes

The logic and protocol analyzer software package combined with the B4661A installation package includes all standard and optional software. Standard features are always available for use. Optional features require the purchase of a license to enable the full functionality of the option. You can obtain a one-time, full-featured 30-day trial license from Keysight.com.
The Keysight B4661A memory analysis software provides four standard software features and four licensed memory analysis options.

Standard software features

- Default configurations for DDR and LPDDR probing solutions for Keysight logic analyzers
- DDR setup assistant
- DDR eye finder/eye scan
- DDR configuration creator

Licensed software options

- DDR decoder with physical address trigger tool (B4661A-1xx)
- LPDDR decoder with physical address trigger tool for LPDDR/2/3 (B4661A-2xx)
- DDR and LPDDR compliance violation analysis toolset (B4661A-3xx)
  - Post-process compliance violation analysis
  - Real-time compliance violation analysis
- DDR3/4 and LPDDR2/3/4 performance analysis (B4661A-4xx)

DDR and LPDDR compatibility for B4661A options

	DDR	DDR2	DDR3	DDR4	LPDDR	LPDDR2	LPDDR3	LPDDR4
DDR decoder with physical address trigger tool (-1xx)	√	√	√	√				
LPDDR decoder (-2xx)					√	√	√	√
DDR and LPDDR compliance violation analysis (-3xx)	√	√	√	√	√	√	√	√
DDR3/4 and LPDDR2/3/4 performance analysis (-4xx)			√	√		√	√	√

Ordering Information

B4661A Memory Analysis Software

The B4661A installation package includes standard and optional licensed software. Standard features are always available for use. Optional licensed features require the purchase of a license to enable the full functionality of the option. You can obtain a one-time full featured, 30-day trial license from Keysight.com.

When ordering, if you request the email delivery option, you will be sent an electronic copy of the Entitlement Certificate so you redeem your license and begin using the software, often on the same day.

1. Select the desired license type

- Fixed perpetual license - the license is locked to the PC where the B4661A Memory Analysis software operates
- Transportable perpetual license - the license is locked to the PC where B4661A Memory Analysis software operates, however the license can be moved. The deletion from one host PC is confirmed prior to issuing a license for another host PC.
- Floating/server perpetual license - the license is locked to a license server from which the B4661A Memory Analysis software automatically checks out the necessary licenses. Licenses are checked back into the server once your analysis session is terminated. Each use of a licensed tool uses a single count of the server license. The count for each server license is:
  - B4661A-1NP server license count = 2
  - B4661A-2NP server license count = 4
  - B4661A-3NP server license count = 4
  - B4661A-4NP server license count = 4

2. Select the desired functionality.

B4661A	Memory analysis software for logic analyzers standard features at no-charge, includes: Default configurations, DDR setup assistant, DDR configuration creator, DDR EyeScan and EyeFinder
Fixed perpetual licenses	
B4661A-1FP	DDR decoder with physical address trigger tool, fixed perpetual license
B4661A-2FP	LPDDR decoder, fixed perpetual license
B4661A-3FP	DDR and LPDDR compliance violation analysis, fixed perpetual license
B4661A-4FP	DDR3/4 and LPDDR2/3/4 performance analysis, fixed perpetual license
Transportable perpetual licenses	
B4661A-1TP	DDR decoder with physical address trigger tool, transportable perpetual license
B4661A-2TP	LPDDR decoder, transportable perpetual license
B4661A-3TP	DDR and LPDDR compliance violation analysis, transportable perpetual license
B4661A-4TP	DDR3/4 and LPDDR2/3/4 performance analysis, transportable perpetual license
Floating/server perpetual licenses	
B4661A-1NP	DDR decoder with physical address trigger tool, network/floating perpetual license
B4661A-2NP	LPDDR decoder, network/floating perpetual license
B4661A-3NP	DDR and LPDDR compliance violation analysis, network/floating perpetual license
B4661A-4NP	DDR3/4 LPDDR2/3/4 performance analysis, network/floating perpetual license

Related Products

The B4661A operates with the following Logic Analyzers modules and probes from Keysight Technologies. Logic analyzer selection criteria includes: logic analyzer specifications and characteristics, maximum DDR technology data rate, and minimum data valid windows of the data eyes at the logic analyzer probe point.

Product	Description
AXIe-based logic analyzers	
U4154B	U4154B 136-channel, 4 Gb/s state, AXIe-based logic analyzer module allowing 3 modules to merge
U4154A	U4154A 136-channel, 4 Gb/s state, AXIe-based logic analyzer module
16850A	16850A Series Portable Logic Analyzers [1]
DDR4 BGA interposers	
W4633A	DDR4 x4/x8, 78 ball, ADD/CMD/DQ, 3.2Gb/s, BGA interposer for logic analyzers
W4631A	DDR4 x16, 96 ball, ADD/CMD/DQ, 3.2Gb/s, BGA interposer for logic analyzers
W4636A	DDR4 x16, 96 ball, ADD/CMD/partial DQ, 2.4Gb/s, BGA interposer for logic analyzers
DDR3 BGA interposers	
W3631A	DDR3 x16 BGA command and data probe for logic analyzer and oscilloscope
W3633A	DDR3 x4/x8 BGA command and data probe for logic analyzer and oscilloscope
Required software	
Logic and protocol analyzer software. Version 6.2 or higher is required. The latest logic and protocol analyzer software is available for download from **www.keysight.com/find/lpa-sw-download**.	

For additional DDR/2/3/4 and LPDDR/2/3/4 probing options, contact your local Keysight representative **www.keysight.com/find/contactus** or refer to the U4154B logic analyzer data sheet, 5992-0180EN.

Information on FuturePlus DIMM and SODIMM interposers for DDR2, DDR3, and DDR4 is available at **www.futureplus.com/DDR3-Memory/keysight-la-support-overview.html.**

For additional analysis software, refer to **www.keysight.com/find/logic-sw-apps.**

1. For DDR3 ADD/CMD analysis up to DDR3 1400 Mb/s (700 MHz clock).

Related Literature

Publication title	Pub number
U4154B 4 Gb/s State Mode Logic Analyzer Module - Data Sheet	5992-0108EN
W4630A Series DDR4 BGA Interposers for Logic Analyzers - Data Sheet	5991-4258EN
16850A Series Portable Logic Analyzers - Data Sheet	5991-2791EN
W3630A Series DDR3 BGA Probes for Logic Analyzers and Oscilloscopes - Data Sheet	5990-3179EN

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www.keysight.com/find/B4661A

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at:
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United Kingdom	0800 0260637

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